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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Artificial Intelligence and Machine Learning **Duration: 3 hrs.**

Course Code: 23AM3ESCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

		UNIT - I	CO	PO	Marks
1	a)	Define computer program. Describe the essential components forming the operational core of a computer system.	CO1	PO1	**05**
	b)	Illustrate the different types of registers in CPU and also provide their purpose.	CO1	PO1	**07**
	c)	Registers R1 and R2 hold decimal values 1200 and 4600, respectively. Analyze the addressing modes and compute the effective address of the source operand for each of the following instructions: i. Load 20(R1),RS ii. Move #3000,RS iii. Store RS,30(R1,R2) iv. Add-(R2),R5 v. Subtract (R1) +, R5	CO2	PO2	**08**
		OR			
2	a)	Elucidate the intricate stages involved in the execution cycle of instructions within the context of a computer system.	CO1	PO2	**07**
	b)	How do basic instruction types operate within computer programming paradigms? Evaluate: (A+B) * (C+D) by considering 3 basic instruction addresses.	CO1	PO3	**09**
	c)	Explain Register Transfer Language notations used to specify the sequence of micro-operations.	CO1	PO1	**04**
		UNIT - II			
3	a)	Illustrate the shift-add-multiplier algorithm through a well-structured flowchart. Apply this method to compute the product of 9 multiplied by 12.	CO1	PO3	**10**

		b)	Write a flowchart that describes the process of performing integer addition and subtraction using signed magnitude representation. Explain the steps involved.	CO1	PO2	**06**
		c)	Perform carry save multiplier for: (1011 * 1101).	CO1	PO3	**04**
			OR			
	4	a)	i. Apply a Booth recording technique to calculate the product of +13 and -6. ii. Perform carry-save addition (CSA) for the binary numbers 101101 (multiplicand) and 111111 (multiplier).	CO1	PO3	**10**
		b)	Outline the sequential steps comprising the division-restoring algorithm. Apply the restoring division algorithm to compute 11 divided by 3.	CO1	PO3	**10**
			UNIT - III			
	5	a)	Distinguish between hardware control unit and micro programmed control unit.	CO2	PO2	**05**
		b)	Describe sequence counter method with an example to illustrate its application.	CO2	PO2	**07**
		c)	Illustrate the mechanism of the Hardwired control unit with a neat labelled diagram.	CO2	PO3	**08**
			OR			
	6	a)	Elaborate on the fundamental components inherent to a microprogrammed control unit. Provide an illustrative example to demonstrate their functionality within control unit architecture.	CO2	PO2	**07**
		b)	Describe different types of semiconductor memory technologies.	CO1	PO1	**06**
		c)	Examine the design factors and architecture of a hypothetical Central Processing Unit. Also explain how Control Unit generates control signals for a simple hypothetical instruction using its control memory.	CO2	PO2	**07**
			UNIT - IV			
	7	a)	Analyze the mechanism for inputting a block of data using interrupt-driven I/O. Provide a detailed explanation with an appropriate diagram to illustrate the process effectively.	CO2	PO2	**07**
		b)	Illustrate the process state transitions with a neat diagram.	CO6	PO2	**06**
		c)	Describe the concept of Direct Memory Access (DMA) with diagram to illustrate its operation.	CO3	PO3	**07**
			OR			
	8	a)	Detail the concept of program-controlled input/output (I/O) within computer systems, elucidating its workings and significance. Provide an example to demonstrate how program-controlled I/O is utilized effectively.	CO2	PO2	**07**

		b)	Elucidate software interrupt and exceptions with an example.	CO2	PO1	**06**
		c)	Explain any two methods of handling interrupts from multiple devices.	CO1	PO1	**07**
			UNIT - V			
	9	a)	Explore the concept of pipelining with various stages of instruction execution and also demonstrate control hazard.	CO3	PO2	**06**
		b)	A family is preparing for a weekend trip by completing multiple loads of laundry, including washing, drying, folding, and organizing clothes. Analyze how these tasks can be optimized using the traditional pipeline concept, focusing on how each stage can be connected and streamlined to reduce delays and improve overall efficiency.	CO**3**	PO**3**	**10**
		c)	Illustrate the data hazard with an example, and explain how it affects the execution of instructions in a computer system.	CO3	PO2	**04**
			OR			
	10	a)	Elucidate the principles and mechanisms underlying Direct Memory Mapping and Associative Memory Mapping.	CO3	PO1	**07**
		b)	Determine the number of page faults incurred using FIFO and LRU page replacement algorithms with a memory capacity of 3 frames, given the page reference sequence: 7,0,1,2,0,3,0,4,2,3,0,3,2,1,2,0,1,7,0,1	CO3	PO3	**08**
		c)	Calculate the average access time experienced by a processor, if a cache hit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 milliseconds.	CO3	PO3	**05**

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