U.S.N.										

B.M.S.College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Artificial Intelligence and Machine Learning **Duration: 3 hrs.**

Course Code: 23AM3ESCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions:1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Explain the basic functional blocks of a computer with neat diagram.	*CO1*	*PO1*	**05**
	b)	Illustrate the instruction execution cycle in detail by considering an instruction: ADD A,B	*CO1*	*PO2*	**07**
	c)	Register R1 and R2 of computer contain the decimal value 1200 and 4600 respectively. Describe the corresponding addressing modes and compute the effective address of the source operand in each of the following instructions: i. Load 20(R1),RS ii. Move #3000,RS iii. Store RS,30(R1,R2) iv. Add-(R2),R5 v. Subtract (R1)+, R5	*CO2*	*PO2*	**08**
		OR			
2	a)	Explain Register Transfer Language notations used to specify the sequence of micro-operations.	*CO1*	*PO1*	**05**
	b)	Illustrate the functions of different types of registers in CPU.	*CO1*	*PO2*	**07**
	c)	Consider the instruction: (A+B) * (C+D) and evaluate it using the following instruction formats: i. three address ii. two address iii. one address iv. zero address	*CO2*	*PO2*	**08**
		UNIT - II			
3	a)	Design an ‘n’ bit carry propagation adder circuit to add ‘K’-‘n’ bit numbers.	*CO2*	*PO2*	**06**

		b)	Perform ((-4) + (-2)) and ((-6) - (-1)) arithmetic operations on signed integers with 4-bit binary representation using 2's complement. And also state whether overflow occurs or not in each case.	*CO2*	*PO2*	**06**
		c)	Write the steps for non–restoring division algorithm. Apply the same on dividend – 8 and divisor – 2.	*CO2*	*PO2*	**08**
			OR			
	4	a)	Design a 4-bit carry look ahead adder logic circuit by considering carry and sum.	*CO2*	*PO2*	**06**
		b)	Describe the 32-bit floating point representation in IEEE standard format using: i. Single precision ii. Double precision	*CO2*	*PO2*	**06**
		c)	i. Write Booth multiplier recoding table. Apply the same to multiply +13 and -6. ii. Perform carry save addition on 101101(Multiplicand) and 111111(Multiplier).	*CO2*	*PO2*	**08**
			UNIT - III			
	5	a)	Explain the hardware control unit with neat diagram.	*CO1*	*PO1*	**06**
		b)	Illustrate the simple hypothetical CPU with an example.	*CO2*	*PO2*	**06**
		c)	Describe the mechanism on micro programmed control unit which is used to implement control unit.	*CO2*	*PO3*	**08**
			OR			
	6	a)	Describe different types of semiconductor memory technologies.	*CO1*	*PO1*	**06**
		b)	Distinguish between hardware control unit and micro programmed control unit.	*CO2*	*PO2*	**06**
		c)	Analyze the sequence counter method in computer programming and also provide its applications with suitable examples.	*CO2*	*PO3*	**08**
			UNIT - IV			
	7	a)	Explain the Direct Memory Access (DMA) with neat diagram. Also elaborate on registers in DMA controller.	*CO1*	*PO1*	**06**
		b)	Distinguish between software interrupts and exceptions with suitable examples.	*CO2*	*PO3*	**06**
		c)	Analyze the mechanism for input a block of data using the following techniques with suitable diagram: i. Programmed I/O ii. Interrupt –driven I/O	*CO2*	*PO3*	**08**
			OR			
	8	a)	Explain any two method of handling interrupts from multiple devices.	*CO1*	*PO1*	**06**

<table>
<tr><td></td><td></td><td>b)</td><td>Distinguish between privileged and non- privileged instructions in computer architecture.</td><td>CO2</td><td>PO3</td><td>06</td></tr>
<tr><td></td><td></td><td>c)</td><td>Consider Alice is designing a high-performance networking device for a data center. Demonstrate how DMA (Direct Memory Access) can efficiently transfer large volumes of data between the network interface and system memory, considering factors such as minimizing CPU involvement and optimizing throughput.</td><td>CO2</td><td>PO3</td><td>08</td></tr>
<tr><td></td><td></td><td></td><td>UNIT - V</td><td></td><td></td><td></td></tr>
<tr><td></td><td>9</td><td>a)</td><td>For a given page reference sequence: 7,0,1,2,0,3,0, 4,2,3,0,3,2,1,2,0,1,7,0,1. Calculate the number of page faults incurred using FIFO and LRU page replacement algorithms with a memory capacity of 3 frames.</td><td>CO2</td><td>PO1</td><td>05</td></tr>
<tr><td></td><td></td><td>b)</td><td>Illustrate occurrence of data hazard and instruction hazard in pipelining.</td><td>CO2</td><td>PO1</td><td>05</td></tr>
<tr><td></td><td></td><td>c)</td><td>Consider the 5 stages of the processor have the following latencies:
<table>
<tr><td></td><td>Fetch</td><td>Decode</td><td>Execute</td><td>Memory</td><td>Writeback</td></tr>
<tr><td>1</td><td>300ps</td><td>400ps</td><td>350ps</td><td>550ps</td><td>100ps</td></tr>
<tr><td>2</td><td>200ps</td><td>150ps</td><td>100ps</td><td>190ps</td><td>140ps</td></tr>
</table>
Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages. Now compute the following:
i. For Non-pipelined processor, compute the cycle time, latency of an instruction and the throughput.
ii. For pipelined processor, compute the cycle time, latency of an instruction and the throughput.
iii. Analyze the efficiency between (i) and (ii) with suitable justification.</td><td>CO2</td><td>PO3</td><td>10</td></tr>
<tr><td></td><td></td><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td></td><td>10</td><td>a)</td><td>Calculate the average access time experienced by a processor, if a cache hit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 milliseconds.</td><td>CO2</td><td>PO1</td><td>05</td></tr>
<tr><td></td><td></td><td>b)</td><td>Illustrate memory interleaving in memory organization with neat diagram.</td><td>CO2</td><td>PO1</td><td>05</td></tr>
<tr><td></td><td></td><td>c)</td><td>A block-set-associate cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words. With this answer the following:
i. Mechanism of set-associative mapping with suitable diagram.
ii. Calculate the number of bits in a main memory address.
iii. Calculate the number of bits in in each of the TAG, SET and WORD fields.</td><td>CO2</td><td>PO3</td><td>10</td></tr>
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