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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2025 Semester End Make-Up Examinations

Programme: B.E. **Semester: III**

Branch: Machine Learning (AI & ML) **Duration: 3 hrs.**

Course Code: 23AM3ESCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Illustrate computer architecture in detail with a diagram.	*CO1*	*PO1*	**07**
	b)	Consider a five stage CPU execution cycle and identify under what stage the following scenarios/instructions hold good with appropriate justification. i. The control unit interprets the opcode and identifies the required operands and operation. ii. ADD AX, [1234h]. iii. MOV [5678h], AX. iv. Add the value from memory to the value in AX.	*CO2*	*PO2*	**08**
	c)	Justify the statement "The Instruction Set Architecture acts as a bridge between software and hardware".	*CO1*	*PO2*	**05**
		OR			
2	a)	Illustrate Traditional Von Neuman Architecture with a diagram and mention the disadvantages of the architecture.	*CO1*	*PO2*	**07**
	b)	Analyze the following instruction and determine valid addressing mode and justify your answer. i. MOV AL, 5. ii. MOV AX, BX. iii. MOV AX, [BX]. v. MOV AX, [BX + SI + 10].	*CO2*	*PO2*	**08**
	c)	Differentiate RISC and CISC Instruction set Architecture.	*CO1*	*PO1*	**05**
		UNIT - II			
3	a)	Describe Fixed point representation by hardware with an example.	*CO1*	*PO2*	**04**
	b)	Apply shift and add method to multiply 9 and 12 using with a 4-bit representation.	*CO2*	*PO1*	**06**
	c)	Write the sequential steps comprising the division-restoring algorithm. Apply the restoring division algorithm to compute 11 divided by 3.	*CO2*	*PO1*	**10**

			OR			
	4	a)	Illustrate 4-bit carry look-ahead adder with a diagram.	*CO1*	*PO1*	**06**
		b)	Apply Booth's algorithm with a 4-bit representation to multiply -5 and -7.	*CO2*	*PO2*	**06**
		c)	Apply Non-Restoring Division for an unsigned integer with a dividend of 11 and a divisor of 3.	*CO2*	*PO2*	**08**
			UNIT - III			
	5	a)	Compare and contrast hardwired and micro-programmed designs with neat circuit diagrams.	*CO1*	*PO1*	**10**
		b)	Illustrate hypothetical computer design with suitable diagram.	*CO1*	*PO2*	**10**
			OR			
	6	a)	Describe state table method and delay element method used in hardwired control design.	*CO1*	*PO1*	**10**
		b)	Illustrate RAM, ROM and Flash memory in semi-conductor memory technologies.	*CO1*	*PO1*	**10**
			UNIT - IV			
	7	a)	Describe Input-output module structure and program-controlled input/output (I/O) module structure with a neat diagram.	*CO1*	*PO1*	**08**
		b)	Analyze the following use cases and justify which appropriate I/O transfer technique is suitable. i. Devices with infrequent or irregular data transfer, like keyboards or mice. ii. Simple systems where hardware or timing constraints make polling acceptable iii. Systems where hardware or timing constraints make polling acceptable.	*CO3*	*PO2*	**06**
		c)	Illustrate the process state transitions with a neat diagram.	*CO3*	*PO2*	**06**
			OR			
	8	a)	Differentiate software and hardware interrupt.	*CO1*		**05**
		b)	Describe DMA in detail with a neat diagram and mention its applications.	*CO1*	*PO2*	**08**
		c)	Explain any two methods of handling interrupts from multiple devices.	*CO1*	*PO1*	**07**
			UNIT - V			
	9	a)	Signify the importance of pipelining in the modern CPU world. Demonstrate 5 stage pipeline process for four instructions that needs to be executed parallelly.	*CO3*	*PO2*	**07**
		b)	What might cause a data hazard in pipelining? Justify. Provide any two solutions for the following instruction set to resolve data hazard (Assume 5 stage pipeline process). I1: ADD R1, R2, R3 I2: SUB R4, R1, R5	*CO3*	*PO1*	**06**

		c)	Define Cache hit and miss. Using FIFO replacement policy calculate page faults and hits for the string 1,3,0,3,5,6 with 3-page frames.	*CO3*	*PO1*	**07**
			OR			
	10	a)	Illustrate the role of cache in memory management with a neat diagram.	*CO1*	*PO1*	**05**
		b)	Illustrate data and control pipeline hazards with an example. Provide solutions for the same.	*CO1*	*PO2*	**07**
		c)	Consider a reference string: 4, 7, 6, 1, 7, 6, 1, 2, 7, 2 and the number of frames in the memory is 3. Find out the number of page faults using FIFO and LRU.	*CO3*	*PO1*	**08**

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