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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Artificial Intelligence and Machine Learning **Duration: 3 hrs.**
Course Code: 23AM3ESCOA **Max Marks: 100**
Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing identification, and appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Illustrate the different phases involved in the Instruction execution cycle	*CO 1*	*PO 1*	**07**
	b)	An integer is stored in the memory. A pointer to this integer is at address 200. Apply memory indirect addressing to increment the number to next address.	*CO 2*	*PO 2*	**07**
	c)	Describe the internal components of a computer with its primary functionalities with a neat diagram.	*CO 1*	*PO 1*	**06**
		UNIT - II			
2	a)	Compare Ripple carry adder with Propagation delay.	*CO 1*	*PO 1*	**06**
	b)	Convert the following decimal number 7.5 to be stored in a 16-bit register with 4-bit after the binary point using 2's complement.	*CO 2*	*PO 2*	**06**
	c)	Consider a scenario where you are working with a computer system that uses the IEEE 754 standard for floating-point representation. Encode the decimal number 1259.125_{10} in single-precision and double-precision.	*CO 2*	*PO 3*	**08**
		OR			
3	a)	Differentiate between restoring and non-restoring division algorithms.	*CO 1*	*PO 1*	**04**
	b)	Describe the working procedure of Booth's algorithm with a neat flow chart and Apply Booth's algorithm to calculate the product of -5 and -7.	*CO 2*	*PO 3*	**08**
	c)	Illustrate the shift-and-add multiplication algorithm by performing the multiplication of the binary numbers 1001 and 1100.	*CO 2*	*PO 3*	**08**
		UNIT - III			
4	a)	Describe the factors influencing the speed and density of semiconductor memory devices.	*CO 1*	*PO 1*	**06**
	b)	How microprogramming contributes to the overall performance of a CPU? Explain.	*CO 2*	*PO 1*	**06**

		c)	Illustrate the mechanism of the hardwired control unit with a neat labeled diagram to ensure the team comprehends the operation.	*CO 1*	*PO 1*	**08**
			UNIT – IV			
	5	a)	Illustrate handling of an interrupt in a computer system during I/O operations.	*CO 1*	*PO 1*	**06**
		b)	Differentiate between the address bus, data bus, and control bus.	*CO 1*	*PO 1*	**06**
		c)	A high-performance graphics card is installed in a computer system. Elucidate how DMA can efficiently transfer image data from the system's main memory to the graphics card's memory for rendering.	*CO 2*	*PO 2*	**08**
			UNIT - V			
	6	a)	Illustrate the concept of structural hazards in CPU pipelining and apply the strategies to mitigate their occurrence.	*CO 1*	*PO 1*	**06**
		b)	Describe the principle of spatial and temporal locality and justify how it influences cache behavior.	*CO 1*	*PO 1*	**06**
		c)	Consider a direct mapped cache of size 16 KB with a block size of 256 bytes. The size of the main memory is 128 KB. Find, 1. The number of bits in the tag 2. Tag directory size.	*CO 2*	*PO 3*	**08**
			OR			
	7	a)	Differentiate between Direct-mapping, Associative mapping & Set-associative mapping.	*CO 1*	*PO 1*	**06**
		b)	Describe a cache hit Ratio with an example and illustrate how to calculate a cache hit ratio.	*CO 2*	*PO1*	**06**
		c)	Consider a reference string: 4, 7, 6, 1, 7, 6, 1, 2, 7, 2. The number of frames in the memory is 3. Find out the number of page faults with respect to: 1. FIFO Page Replacement Algorithm 2. LRU Page Replacement Algorithm	*CO 2*	*PO 2*	**08**

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