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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E.   Semester: III
Branch: Artificial Intelligence and Machine Learning   Duration: 3 hrs.
Course Code: 23AM3ESCOA   Max Marks: 100
Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

				CO	PO	Marks
			UNIT - I			
1	a)		Outline the significance of registers present in computer.	CO1	PO1	**6**
	b)		List and explain different instruction formats.	CO1	PO1	**6**
	c)		Provide the RTL notation for memory operations, detailing the sequence of micro-operations involved and the transfer of data between the specified components of the computer system.	CO2	PO2	**8**
			UNIT - II			
2	a)		Demonstrate how does the structure of a Carry Look Ahead Adder with its design to contribute its efficiency in terms of reducing the propagation delay and enabling parallelism compared to ripple carry adders.	CO2	PO2	**10**
	b)		Imagine Bob is working with a computer system that uses IEEE 754 standard 32-bit floating point representation. He needs to convert the decimal numbers 0.09375 and 1.025 into its corresponding 32-bit floating-point single precision IEEE 754 format. Outline the step-by-step process involved in this conversion, including how the sign bit, exponent, and mantissa are determined.	CO2	PO3	**10**
			OR			
3	a)		Illustrate the detailed process of employing the restoring division algorithm to compute the division of 9 by 3.	CO2	PO2	**10**
	b)		Apply Booth's algorithm to calculate the product of: 1) - 07 (multiplicand) and 03 (multiplier) 2) 0111 * 1011	CO2	PO3	**10**
			UNIT - III			
4	a)		Elucidate two distinct types of semiconductor memory, detailing their unique characteristics, and advantages compared to alternative memory technologies.	CO3	PO2	**7**

		b)	Differentiate between Hardwired and micro programmable control unit	*CO3*	*PO2*	**5**
		c)	Illustrate how microprogrammed control units play a crucial role in achieving computational tasks efficiently.	*CO2*	*PO2*	**8**
			UNIT - IV			
	5	a)	Elucidate software interrupt and exceptions with example	*CO2*	*PO1*	**6**
		b)	Illustrate the structure of a system bus including its components and application within a computer system.	*CO1*	*PO1*	**6**
		c)	Demonstrate how DMA (Direct Memory Access) can efficiently transfer large volumes of data between the network interface and system memory, considering factors such as minimizing CPU involvement and optimizing throughput.	*CO2*	*PO2*	**8**
			UNIT - V			
	6	a)	Differentiate between cache hits and cache misses, and explain how data flows between the cache and main memory	*CO1*	*PO1*	**6**
		b)	Describe the stages involved in a typical instruction pipeline and explain the function of each stage.	*CO2*	*PO2*	**6**
		c)	Apply FIFO and LRU Page Replacement algorithms on the following page reference string 7,1,0,2,0,3,0,4,2,1,0 for a memory with 3 frames and calculate the total occurrences of page faults and page hits.	*CO2*	*PO3*	**8**
			OR			
	7	a)	Explain how structural hazards arise in pipelined architectures and provide examples of situations where they can occur.	*CO2*	*PO2*	**6**
		b)	Calculate the average access time experienced by a processor, if a cache hit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 milliseconds	*CO2*	*PO3*	**6**
		c)	Elucidate the principles and mechanisms underlying Direct Memory Mapping and Associative Memory Mapping.	*CO2*	*PO1*	**8**

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