U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Artificial Intelligence & Machine Learning **Duration: 3 hrs.**

Course Code: 20AM3ESLDA **Max Marks: 100**

Course: LOGIC DESIGN AND COMPUTER ARCHITECTURE

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Simplify the following Boolean expression using the Karnaugh Map (K-map) method and the entered variable technique: $Y=F(A,B,C,D)= \pi M(0,1,2,4,5,10).d(8,9,11,12,13,15)$ Provide the simplified Sum-of-Products (SOP) form and a gate diagram for the simplified Boolean expression using NOR-NOR gates.	*CO1*	*PO2*	**10**
	b)	What are universal gates? Demonstrate how basic logic gates (AND, OR, NOT) can be realized using only NAND gates.	*CO1*	*PO1*	**05**
	c)	Explain the working of a parity checker using suitable examples. Illustrate how they can be used in error detection and correction.	*CO2*	*PO1*	**05**
		OR			
2	a)	Design a parity generator for a 4-bit data input. Explain the steps involved in generating both even and odd parity.	*CO2*	*PO3*	**04**
	b)	Use the Quine-McClusky method to simplify the Boolean function: $F(A,B,C,D)=\Sigma m(1,2,4,5,6,8,9,10,12)$ Find the prime implicants and write the simplified Boolean expression. Implement the simplified function using NAND gates.	*CO1*	*PO3*	**10**
	c)	Using a 3-to-8 decoder and a multi-input OR gate, show how the following Boolean expressions can be realized: • $F_1(A,B,C)=\Sigma m(0,4,6)$ • $F_2(A,B,C)=\Sigma m(0,5)$ • $F_3(A,B,C)=\Sigma m(1,2,3,7)$ Explain how the decoder and OR gates work together in implementing the above functions.	*CO2*	*PO3*	**06**

			UNIT - II			
	3	a)	Design an SR flip-flop using NOR gates. Write the truth table and the characteristic equation of the SR flip-flop.	*CO3*	*PO3*	**08**
		b)	Design an Asynchronous 3-bit up-counter using JK flip-flops. Draw the counter diagram and show the state transitions for each clock pulse.	*CO3*	*PO3*	**08**
		c)	Explain the operation of a D flip-flop. Derive its characteristic equation.	*CO2*	*PO1*	**04**
			OR			
	4	a)	Explain the operation of a JK flip-flop. Draw its timing diagram for each possible combination of J and K inputs (00, 01, 10, 11).	*CO2*	*PO1*	**07**
		b)	Design a 4-bit parallel-in, parallel-out shift register using D flip-flops**.** Explain its working with waveforms.	*CO2*	*PO3*	**07**
		c)	Derive the characteristic equation of a T flip-flop and explain its working for input combinations T=0T = 0T=0 and T=1T = 1T=1.	*CO2*	*PO3*	**06**
			UNIT - III			
	5	a)	Given a system with a data bus of 16 bits, explain how data is transferred between the CPU and memory when the CPU needs to fetch a 32-bit word. Illustrate with a diagram.	*CO3*	*PO3*	**07**
		b)	What is performance measurement in computer systems? Describe how the overall SPEC rating is calculated for a computer using a given program suite.	*CO2*	*PO1*	**07**
		c)	Describe direct addressing mode and immediate addressing mode with examples.	*CO2*	*PO1*	**06**
			OR			
	6	a)	Use immediate addressing and indirect addressing to write assembly language instructions that load the value 25 into Register R1 and the value stored at memory location 5000 into Register R2.	*CO2*	*PO3*	**08**
		b)	Calculate the effective address of the operand for the following instruction: Load 30(R2), R3, where R2 = 4500. Show your steps clearly.	*CO3*	*PO3*	**06**
		c)	Explain the concept of a **bus** in computer systems. What are the different types of buses, and what roles do they play?	*CO2*	*PO1*	**06**
			UNIT - IV			
	7	a)	Explain the concept of vectored interrupts and how they differ from non-vectored interrupts**.**	*CO3*	*PO1*	**05**

		b)	Explain how signed numbers are represented in 2's complement form**.** Perform the addition of (+25) and (-15) using 2's complement representation.	*CO3*	*PO1*	**05**
		c)	Design a 4-bit carry-lookahead adder and explain its working with a block diagram.	*CO3*	*PO3*	**10**
			OR			
	8	a)	Describe the process of interrupt handling and the role of interrupt service routines (ISRs)**.**	*CO1*	*PO1*	**06**
		b)	Perform multiplication of the following signed numbers using Booth's algorithm: i. (+14)×(−5) ii. (−12)×(−11) iii. (14)×(−6)	*CO3*	*PO3*	**08**
		c)	Compare and contrast the following I/O techniques: Programmed I/O**,** Interrupt-driven I/O, and Direct Memory Access (DMA)**.**	*CO2*	*PO2*	**06**
			UNIT - V			
	9	a)	Differentiate hardwired control and microprogrammed control units. Highlight their advantages and disadvantages.	*CO2*	*PO2*	**10**
		b)	Define memory hierarchy in a computer system. Explain the significance of cache memory in improving system performance.	*CO2*	*PO1*	**05**
		c)	What is a single-bus organization**?** Briefly explain its advantages and disadvantages	*CO3*	*PO1*	**05**
			OR			
	10	a)	Discuss the concept of cache memory. Explain associative mapping with the help of a diagram and examples.	*CO2*	*PO1*	**10**
		b)	Compare single-bus**,** two-bus**,** and three-bus organizations in terms of data transfer efficiency and complexity.	*CO3*	*PO2*	**05**
		c)	What is a microinstruction? Briefly explain its role in a microprogrammed control unit.	*CO3*	*PO1*	**05**

****