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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2023 Supplementary Examinations

Programme: B.E.

Semester: III

Branch: Artificial Intelligence and Machine Learning

Duration: 3 hrs.

Course Code: 22AM3ESLDA

Max Marks: 100

Course: Logic Design and Computer Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Simplify the following Boolean function using Quine McCluskey method to find the prime implicants and Essential prime implicants. 10

$$f(a,b,c,d) = \Sigma m(0,2,3,4,8,10,12,13,14)$$

b) Find the prime implicants and essential prime implicants for the given function using K-map. 5

$$f(a,b,c,d) = \pi M(0,3,4,5,6,7,11,15) \cdot \pi d(2,14)$$

c) Illustrate the working of Even Parity Generator with a diagram. 5

UNIT - II

2 a) Illustrate the working of SR Flipflop with the help of a circuit diagram and a truth table. 6

b) Design Mod-8 synchronous UP Counter Using JK Flipflop. 10

c) Consider a 3-bit Johnson counter with input data word as 001, determine all definite states of Johnson counter. 4

OR

3 a) Find the characteristic equations of:
 i) SR flip-flop
 ii) D flip-flop
 iii) JK flip-flop
 iv) T flip-flop 8

b) Design a 4-bit PISO shift register using D Flip Flop. 6

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

c) Realize JK master slave flip-flop with a neat circuit, truth table and timing diagram. **6**

UNIT - III

4 a) Illustrate the Top-Level View of various Computer Components with a diagram. **6**

b) Explain the Instruction Cycle State Diagram. **6**

c) Describe the Bus Interconnection Scheme. **8**

UNIT - IV

5 a) Describe Direct- Mapping Cache Organization with a neat diagram. **4**

b) Given multiplicand $A = -9$, and multiplier $B = -13$, perform the multiplication of A and B using Booth's Multiplication Algorithm. **6**

c) Show with a neat flow diagram the programmed I/O and interrupt driven I/O as part of techniques for input of a block of data. **10**

OR

6 a) Illustrate simple interrupt processing techniques with a neat diagram. **6**

b) Describe Memory hierarchy with a diagram. **6**

c) Illustrate the flowchart for addition and subtraction and explain how an overflow occurs with an example. **8**

UNIT - V

7 a) Differentiate between a hardwired implementation and a micro programmed implementation of a control unit. **6**

b) Illustrate the following addressing modes with an example.

- i. Immediate Addressing
- ii. Direct Addressing
- iii. Indirect Addressing
- iv. Register Addressing
- v. Register Indirect Addressing

c) Mention the advantages and disadvantages of using a variable-length instruction format. **4**
