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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Artificial Intelligence and Machine Learning **Duration: 3 hrs.**
Course Code: 22AM3ESLDA **Max Marks: 100**
Course: Logic Design and Computer Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Simplify the following SOP expression using K-map and implement the reduced expression using only NAND gates. **7**

$F(a,b,c,d) = \sum m(0,4,6,8,10,11,12) + d(1,2,3,9)$

b) Minimize the given SOP function using Tabular Quine McClusky method. **8**

$F(a,b,c,d) = \sum m(0,1,10,11,13,15) + d(2,3,12,14)$

c) Design 8:1 Multiplexer using only 2:1 Multiplexers. **5**

UNIT - II

2 a) Illustrate the working of Master- Slave JK flip-flop With the help of logic diagram, truth table and timing diagram. **8**

b) Derive the characteristic equation of D, T, SR, and JK Flipflops. **7**

c) Construct table for switch tail counter with initial state 1000. Draw the circuit and timing diagram. **5**

OR

3 a) Illustrate the working principle of Serial In Serial Out Shift Register with the help of the diagram and truth table. **7**

b) Design a random synchronous counter for the following sequence using JK flipflops. **8**

$0 \rightarrow 3 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 7 \rightarrow 0$

c) Draw the state transition diagram of D, T, SR and JK flip flops with excitation tables. **5**

UNIT - III

4	a)	Describe the structure of IAS computer giving the significance of each component.	**8**
	b)	Illustrate the states involved in an instruction cycle by considering Instruction Cycle state diagram.	**7**
	c)	Explain Bus Interconnection scheme with neat diagram.	**5**

UNIT - IV

5	a)	Describe Set-Associative memory mapping technique with neat a diagram.	**8**
	b)	Illustrate any two interrupt priority schemes with a neat diagram.	**6**
	c)	List the steps involved in handling interrupt request from a single device.	**6**

OR

6	a)	Design carry-look ahead that helps to perform fast addition.	**7**
	b)	Describe the implementation of sequential circuit multiplier with an example.	**8**
	c)	Apply Booth's Algorithm to perform Multiplication of (+23) * (-9).	**5**

UNIT - V

7	a)	Discuss Shift and Rotate operations with an example.	**6**
	b)	List the Basic Addressing Modes and explain any four of them with an example of each.	**8**
	c)	Illustrate the working of Micro programmed control unit with a neat diagram.	**6**

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