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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Artificial Intelligence and Machine Learning **Duration: 3 hrs.**

Course Code: 22AM3ESLDA **Max Marks: 100**

Course: Logic Design and Computer Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Analyze how a 4-to-1 multiplexer can be used to implement any arbitrary 2-variable Boolean function. Explain the role of select lines and data inputs in realizing the function, and illustrate with an example.	*1*	*2*	**10**
	b)	Using a 4-variable Karnaugh map, simplify the following Boolean function: $F(A, B, C, D) = \Sigma(0, 2, 5, 7, 8, 10, 13, 15)$. Draw the K-map, group the minterms, and derive the simplified Boolean expression.	*1*	*3*	**10**
		OR			
2	a)	Given a logic circuit built using basic gates (AND, OR, NOT), analyze its behavior under both positive and negative logic conventions. How does the interpretation of logic levels affect the function of the circuit? Support your answer with truth tables and logic diagrams.	*1*	*2*	**10**
	b)	Design a 1-of-16 decoder using two 3-to-8 decoders and basic logic gates. Show the block diagram and explain how the enable signals are used to achieve the required functionality.	*1*	*3*	**10**
		UNIT - II			
3	a)	Show that a JK flip-flop can be converted to a D flip flop with an inverter between J and K.	*1*	*2*	**8**
	b)	Design a full adder circuit using basic logic gates. Use the truth table to derive the expressions for Sum and Carry, and then draw the corresponding logic diagram.	*1*	*3*	**12**
		OR			

	4	a)	Analyze the working of a master-slave JK flip-flop with respect to clock transitions. How does it prevent race-around conditions compared to a simple JK flip-flop? Support your explanation with timing diagrams.	*1*	*2*	**10**
		b)	Design a 3-bit up counter using both asynchronous and synchronous counter configurations. Show the circuit diagrams and explain how the timing of the flip-flops differs between the two designs.	*1*	*3*	**10**
			UNIT - III			
	5	a)	Analyze the role of various functional units in a digital computer system using a labeled diagram. How do these units interact to perform operations, particularly when handling signed number representations? Illustrate with an example.	*2*	*2*	**10**
		b)	Explain the role of bus interconnection in a computer system. How do control, data, and address buses coordinate to facilitate communication among CPU, memory, and I/O devices? Compare single-bus and multiple-bus structures in terms of performance, cost, and complexity.	*2*	*1*	**10**
			OR			
	6	a)	Analyze the different interconnection structures used to link major components of a computer system. How do bus-based, point-to-point, and crossbar interconnections impact system performance, scalability, and complexity	*2*	*2*	**10**
		b)	Briefly describe the evolution of computer systems from early mechanical and vacuum tube machines to modern microprocessor-based systems. How have advancements in hardware technology, instruction set architecture, and processing capabilities influenced the development and continued relevance of the x86 family.	*2*	*1*	**10**
			UNIT - IV			
	7	a)	Analyze the memory hierarchy of a computer system by drawing its block diagram and comparing different memory types (registers, cache, main memory, and secondary storage) in terms of size, access speed, and cost per bit. How do these factors influence data access and overall system performance	*2*	*2*	**10**
		b)	Perform the addition and subtraction of the following signed binary numbers using 2's complement representation: (+25) and (–12). Show all steps including binary conversion, 2’s complement computation, and final result interpretation.	*3*	*3*	**10**
			OR			

	8	a)	Compare and analyze the three cache mapping techniques—associative mapping, direct mapping, and set-associative mapping—in terms of address structure, hardware complexity, speed, and hit/miss ratio. How does each method impact overall system performance	*2*	*2*	**10**
		b)	Using the shift-and-add method, perform the binary multiplication of two positive 4-bit numbers: 9 (1001) and 3 (0011). Show each step of the partial products and the final result.	*3*	*3*	**10**
			UNIT - V			
	9	a)	Given the following instruction: MOV R1, [R2 + 4], identify the addressing mode used and explain how the effective address is calculated. Then, provide one example each for immediate, direct, indirect, register, and indexed addressing modes.	*3*	*3*	**12**
		b)	Analyze the functioning of a hardwired control unit in a processor. Elaborate on how it generates control signals based on instruction opcodes.	*3*	*2*	**8**
			OR			
	10	a)	Given a 32-bit instruction format where the opcode takes 6 bits, the source and destination registers take 5 bits each, and the remaining bits are used for the immediate value or address: a) Draw the instruction format layout. b) Determine the maximum value that can be represented in the immediate field. c) Construct a sample instruction using this format and explain each field.	*3*	*3*	**12**
		b)	Analyze the working of a microprogrammed control unit. Explain how does the control store and control address register contribute to instruction execution.	*3*	*2*	**8**

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