

# B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

## May 2023 Semester End Main Examinations

**Programme: B.E.**

**Branch: Artificial Intelligence and Machine Learning**

**Course Code: 22AM3ESLDA**

**Course: Logic Design and Computer Architecture**

**Semester: III**

**Duration: 3 hrs.**

**Max Marks: 100**

**Date: 17.05.2023**

**Instructions:** 1. Answer any FIVE full questions, choosing one full question from each unit.  
2. Missing data, if any, may be suitably assumed.

### UNIT - I

- 1 a) What are universal gates? Realize basic gates using only NOR gates. **4**
- b) Simplify the following expression using K-map and implement the simplified expression using NAND gates. **4**  
 $F(A,B,C,D) = \sum m(0,1, 2, 4, 5,6, 8,9,10,12,13).$
- c) Realize the following function using tabular Quine-McClusky method, and find the prime implicants. **8**  
 $F(A,B,C,D) = \sum m(0,1,2,5,6,7,8,9,10,14).$
- d) Show how using a 3-to-8 decoder and multi-input OR gates for the following Boolean expressions can be realized simultaneously. **4**  
 $F_1(A, B, C) = \sum m(0, 4, 6);$   
 $F_2(A, B, C) = \sum m(0, 5);$   
 $F_3(A, B, C) = \sum m(1, 2, 3, 7)$

### UNIT - II

- 2 a) Write the characteristic equation of i) SR Flip-Flop ii) D Flip-Flop **10**  
 iii) JK Flip-Flop iv) T Flip-flop.
- b) A fictitious flip-flop with two inputs A and B functions like this. For AB= 00 and 11 the output becomes 0 and 1 respectively. For AB= 01, flip-flop retains previous output while output complements for AB= 10. Draw the truth table and excitation table of this flip-flop. **4**
- c) Design a sequential circuit with two D Flip-Flops, A and B, and one input x. When x = 0, then the state of the circuit remains the same. When x = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats. **6**

**OR**

**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

- |   |    |   |   |
|---|----|---|---|
| 3 | a) | Design 4-bit parallel in/serial out shift register using D-Flip flop. | 4 |
|   | b) | Design 4-bit using Switched-Tail Counter D-Flip flop.                 | 8 |
|   | c) | Design 3bit Up-down serial counter using NAND gate and JK Flip flop.  | 8 |

### UNIT - III

- |   |    |  |   |
|---|----|--|---|
| 4 | a) | On the IAS, describe the process that the CPU must undertake to read a value from memory and to write a value to memory in terms of what is put into the MAR, MBR, address bus, data bus, and control bus.   | 6 |
|   | b) | While browsing at Billy Bob's computer store, you overhear a customer asking Billy Bob what is the fastest computer in the store that he can buy. Billy Bob replies, "You're looking at our Macintoshes. The fastest Mac we have runs at a clock speed of 1.2 gigahertz. If you really want the fastest machine, you should buy our 2.4-gigahertz Intel Pentium IV instead." Is Billy Bob correct? What would you say to help this customer? | 6 |
|   | c) | Illustrate the basic instruction cycle with a neat diagram.  | 8 |

### UNIT - IV

- |   |    |  |    |
|---|----|--|----|
| 5 | a) | Illustrate direct, associative and set-associative cache mapping techniques with a neat diagram.                         | 10 |
|   | b) | Define Interrupt and explain the different mechanisms of handling multiple devices using interrupts with a neat diagram. | 10 |

### OR

- |   |    |  |    |
|---|----|--|----|
| 6 | a) | Write Sequential multiplication algorithm and apply it on an example.                                | 10 |
|   | b) | Write Booth Algorithm and provide Booth recoding table .Multiply (-13) * (-6) using Booth algorithm. | 10 |

### UNIT - V

- |   |    |   |    |
|---|----|---|----|
| 7 | a) | Illustrate the different types of instruction formats .Write a program to execute $Y = (A - B) / (C + (D * E))$ using different instruction formats.  | 10 |
|   | b) | Describe the different types Addressing modes and explain the effective address calculation performed in each of the addressing mode with an example. | 10 |

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