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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**

Branch: Artificial Intelligence and Machine Learning **Duration: 3 hrs.**

Course Code: 24AM6PCPAG / 24AM6PCPAP **Max Marks: 100**

Course: Parallel Architectures and Programming

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Elaborate the contrasts between serial computing and parallel computing with a neat diagram.	*CO1*	*PO1*	**06**
	b)		Illustrate the structure of Von Neumann architecture with a block diagram.	*CO1*	*PO1*	**06**
	c)		Elucidate how Flynn's taxonomy categorizes parallel computing architectures based on instruction and data streams?	*CO1*	*PO1*	**08**
			OR			

2	a)		Consider a simple pipelined processor with five stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Write Back (WB), and Memory (MEM). Each instruction takes one clock cycle to complete each stage.
			Instructions in the pipeline are given below:
			ADD R1, R2, R3
			SUB R4, R1, R5
			i) Use instruction space time diagram to Identify the hazard present in the pipeline.
			ii) Resolve the identified hazard using suitable method.
				CO1	*PO3*	**07**

	b)		Derive Amdahl's speedup equation. An examination of a program has revealed a speedup of 3 when executed on 4 cores. Determine the serial fraction according to Amdahl's and Gustafson's laws.	*CO1*	*PO3*	**07**
	c)		Explain how Feng's classification is used to categorize and optimize the processing tasks in the system.	*CO1*	*PO1*	**06**
			UNIT - II			
3	a)		Explain how optimal load control in a multiprogrammed multiprocessing virtual memory system ensures efficient utilization of CPUs and I/O resources.	*CO1*	*PO1*	**07**

	b)	Explain virtual to real address translation using page map.	*CO1*	*PO1*	**07**
	c)	Explain namespace and memory space in virtual memory.	*CO1*	*PO1*	**06**
		OR			
4	a)	Explain virtual memory system and three main types of locality of reference with a suitable example.	*CO1*	*PO1*	**06**
	b)	Discuss three different policies available for placement of a memory block in the cache.	*CO1*	*PO1*	**06**
	c)	Elaborate the basic operations of cache memory with a simplified flowchart of cache operation of a fetch.	*CO1*	*PO1*	**08**
		UNIT - III			
5	a)	Explicate the principles of basic linear pipelining with a neat sketch.	*CO3*	*PO1*	**06**
	b)	List pipeline classification schemes, elaborate the processor pipelining scheme proposed by Li and Ramamoorthy.	*CO3*	*PO1*	**07**
	c)	For the given sequence of stages draw the reservation table and find the forbidden latency. Sa, Sc, Sa, Sa, Sc, Sb	*CO3*	*PO3*	**07**
		OR			
6	a)	Consider the following pipeline reservation table and answer the following: clock cycles / Stages 1 2 3 4 5 6 7 8 S1: x x S2: x x S3: x x x i) What are the forbidden latencies? ii) Draw the state transition diagram. iii) List all the simple cycles and greedy cycles. iv) Determine the minimal average latency.	*CO3*	*PO4*	**10**
	b)	Perform 4-Stage floating point for the given A and B values. A= $0.9504 * 10^3$ B= $0.8200 * 10^2$	*CO3*	*PO4*	**05**
	c)	What is reservation table? With a neat diagram explain 3 stage non-linear pipeline.	*CO3*	*PO1*	**05**

			UNIT - IV			
	7	a)	How does parallelism differ between GPUs & CPUs, and what are the key factors that contribute to this distinction?	*CO2*	*PO1*	**06**
		b)	Provide a neat diagram and explain the key components of the NVIDIA GT200 architecture.	*CO2*	*PO1*	**08**
		c)	With a neat sketch explain the process flow in CUDA.	*CO2*	*PO1*	**06**
			OR			
	8	a)	With neat sketches explain the concepts of threads, grids, and blocks in CUDA, and how computations are divided into threads to facilitate parallel processing?	*CO2*	*PO1*	**10**
		b)	Elucidate the memory hierarchy along with its characteristics to address the diverse requirements of GPU workloads.	*CO2*	*PO1*	**10**
			UNIT - V			
	9	a)	Explain the steps to execute a CUDA program and importance of _global_declaration specifier.	*CO2*	*PO1*	**07**
		b)	Explain the benefits and limitations of CUDA.	*CO2*	*PO1*	**06**
		c)	With a neat sketch explain the architecture of CUDA.	*CO2*	*PO1*	**07**
			OR			
	10	a)	Write and explain a CUDA program to add two matrices considering multi-dimensional blockIdx, threadIdx and blockDim.	*CO3*	*PO3*	**10**
		b)	Explain the information available to each thread while computing one element of an array, in 1-dimensional and 2-dimensional grid.	*CO3*	*PO3*	**10**

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