

U.S.N.

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

October 2024 Supplementary Examinations**Programme: B.E.****Branch: CSE (ICB) / CSE(DS) / AI&DS****Course Code: 23DC3ESCOA****Course: Computer Organization and Architecture****Semester: III****Duration: 3 hrs.****Max Marks: 100**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.			UNIT - I	CO	PO	Marks
	1	a)	Identify different functional units of a Digital Computer and explain with a neat diagram.	CO1	PO1	06
		b)	Utilizing the connection between processor and memory, explain basic operational concepts.	CO1	PO1	07
		c)	With neat representation explain Little-Endian and Big-Endian schemes.	CO1	PO1	07
			UNIT - II			
	2	a)	Illustrates how the keyboard and display devices are connected to the processor with neat diagram.	CO1	PO1	10
		b)	Construct an I/O interface for an input device and explain	CO1	PO1	10
			UNIT - III			
	3	a)	Construct internal organization of a 32M x 8 dynamic memory Chip	CO3	PO3	10
		b)	What is the necessity of DMA? Explain DMA and possible registers used in DMA interface.	CO3	PO3	10
			OR			
	4	a)	Identify and explain the 3 different Memory mapping functions	CO3	PO3	10
		b)	With a neat diagram explain Virtual Memory address translation	CO3	PO3	10
			UNIT - IV			
	5	a)	Design 4-bit carry-look ahead adder circuit	CO3	PO3	10
		b)	Explain sequential circuit binary multiplier with a neat block diagram and an example.	CO3	PO3	10
			OR			
	6	a)	Consider M=13 and Q= -6, solve using bit pair recoding multiplier method. Also show multiplicand selection decision table.	CO3	PO3	10

		b)	Illustrate restoring and non restoring division with suitable examples	CO3	PO3	10
			UNIT - V			
	7	a)	With a neat diagram, demonstrate the working of hardwired control.	CO2	PO2	08
		b)	List the steps needed to execute the instruction Load R5, X(R7)	CO2	PO2	06
		c)	Elucidate the four phases in the evolution of microprocessor design.	CO2	PO2	06

SUPPLEMENTARY EXAMS 2024