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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: CSE (ICB) / CSE(DS) / AI&DS **Duration: 3 hrs.**

Course Code: 23DC3ESCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Elucidate the functional units of a computer with a neat diagram.	*CO1*	*PO1*	**06**
	b)	You are a computer architect working on designing a new processor for a cutting-edge computer system. Your team is discussing the various addressing modes that the processor should support to enhance its versatility. Illustrate the various addressing modes with example code.	*CO2*	*PO2*	**07**
	c)	With a neat diagram, explain the processor memory interface and the various types of registers associated with it.	*CO1*	*PO1*	**07**
		UNIT - II			
2	a)	Write an assembly program to add 'N' numbers and store the final answer in a register.	*CO3*	*PO3*	**06**
	b)	With a neat diagram, explain the working of interrupts.	*CO1*	*PO1*	**07**
	c)	Illustrate the bus arbitration process by considering the case where a single bus is the shared resource.	*CO2*	*PO2*	**07**
		UNIT - III			
3	a)	Construct a block diagram and explain the organization of bit cells in Memory Chips.	*CO1*	*PO1*	**07**
	b)	Outline the significance of registers used in the DMA Controller to carry out the transfer of data block directly between the external device and main memory.	*CO1*	*PO1*	**08**
	c)	Given an 8-bit binary number- 10101101, Perform the following operations where shift size=3: i)Logical Shift Left ii) Arithmetic Shift Right iii)Arithmetic Shift Left iv) Logical Shift Right v) Rotate Right with Carry	*CO3*	*PO3*	**05**

			OR			
	4	a)	Considering the hierarchical nature of memory, analyze your strategy for minimizing data movement between different levels of the memory hierarchy to reduce latency and improve overall system performance.	*CO2*	*PO2*	**06**
		b)	Discuss the Translation Lookaside Buffer (TLB) and its importance in speeding up the address translation process.	*CO1*	*PO1*	**07**
		c)	Design a 2M × 32 memory module using 512K × 8 static memory chips.	*CO3*	*PO3*	**07**
			UNIT - IV			
	5	a)	Multiply 42(multiplicand) with 63(multiplier) using the 3-2 carry-save reducers method.	*CO1*	*PO1*	**08**
		b)	Apply Booth's algorithm to multiply the following pair of numbers A=+19 B= +12	*CO1*	*PO1*	**06**
		c)	Apply Bit Pair Recoding algorithm to multiply M(multiplicand)=+13 and Q(multiplier)=-6	*CO1*	*PO1*	**06**
			OR			
	6	a)	Illustrate the workings of a sequential circuit multiplier with a diagram.	*CO1*	*PO1*	**06**
		b)	Given the Dividend X = 17 and Divisor Y = 3, Solve the given problem using Non-Restoring Division.	*CO2*	*PO2*	**07**
		c)	Design and describe the working of a 4-bit carry look-ahead adder.	*CO3*	*PO3*	**07**
			UNIT - V			
	7	a)	Demonstrate the working of hardwired control organization with a schematic diagram.	*CO1*	*PO1*	**06**
		b)	Give a detailed description for Flynn's taxonomy of Parallel Architecture.	*CO1*	*PO1*	**06**
		c)	Elaborate on the data path organization in a computer with relevant diagrams.	*CO1*	*PO1*	**08**

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