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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: CSE(DS)/AI & DS/CSE(IoT) **Duration: 3 hrs.**

Course Code: 23DC3ESCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Identify the type of addressing mode for each of the given instructions and explain the same. a) Add R2, #2000 b) Mov R7, 50(R6) c) Store (R2), A d) Add R5, LOCA	*CO2*	*PO2*	**8**
	b)	Represent **0100000 10110011 01001111 11110000** in Big-Endian and Little-Endian Formats.	*CO1*	*PO1*	**6**
	c)	Analyze the steps needed for fetching and executing the instructions by illustrating the connections between processor and the main memory.	*CO2*	*PO2*	**6**
		OR			
2	a)	Identify the steps performed by the processor in fetching and executing the given instructions. i) Load R4, B ii) ADD R4, R5, R6	*CO2*	*PO2*	**8**
	b)	Distinguish between straight line sequencing and branching with examples.	*CO1*	*PO1*	**6**
	c)	Convert the following pairs of decimal numbers to 4 bit signed 2's complement binary numbers and subtract them. State whether or not overflow occurs. i) -3 and -7 ii) +2 and +4	*CO1*	*PO1*	**6**
		UNIT - II			
3	a)	Design and interpret the timing diagram for Synchronous and Asynchronous Bus Input operations.	*CO1*	*PO1*	**10**

		b)	Subroutine ADD performs addition of N numbers. Analyze the different ways, parameters can be passed to a subroutine. Justify your answer with necessary code.	*CO1*	*PO1*	**10**
			OR			
	4	a)	Write an Assembly Language Program to read a line from the keyboard, store in the memory and print it on the display.	*CO1*	*PO1*	**6**
		b)	Device1, Device2 and Device3 are connected to the processor. If all the devices send simultaneous requests to the processor, explain the techniques used by the processor to identify the device.	*CO1*	*PO1*	**9**
		c)	Identify the need for arbitration and explain with a neat diagram.	*CO1*	*PO1*	**5**
			UNIT - III			
	5	a)	Design Direct Mapping and Associative mapping functions, given a cache consisting of 128 blocks of 16 words each and memory with 4K blocks of 16 words each.	*CO3*	*PO3*	**10**
		b)	With a neat diagram explain virtual memory organization.	*CO1*	*PO1*	**5**
		c)	A company wants to transfer large amount of data efficiently from an external storage device to the hard disk. Identify the technique used by the processor to transfer the huge amount of data.	*CO2*	*PO2*	**5**
			OR			
	6	a)	Design a Memory of 2M x 32 using 512K x 8 static memory chips. Analyze the number of chips and the address lines needed to design the above memory with a diagram.	*CO3*	*PO3*	**10**
		b)	With a neat diagram explain the memory hierarchy.	*CO1*	*PO1*	**6**
		c)	Differentiate between Write Through and Write Back in Cache	*CO1*	*PO1*	**4**
			UNIT - IV			
	7	a)	Design an Addition and Subtraction circuit and validate your design is correct by performing addition and subtraction for the given below data: Addition where X = 4 and Y = 2 Subtraction where X = -2 and Y = 3	*CO3*	*PO3*	**10**
		b)	Given Dividend A = 11100 and Divisor B = 00101 solve using Non-Restoring Division. Also write the algorithm for Non-Restoring Division and highlight the advantage of using it.	*CO1*	*PO1*	**10**
			OR			
	8	a)	Multiply the pair of signed 2's complement number using Booth's Algorithm and Bit Pair Recoding. Verify the result obtained. Multiplicand A = 010111 Multiplier B = 110110	*CO1*	*PO1*	**10**

		b)	Given the Multiplicand 1101 and Multiplier 1011. Illustrate with a diagram and explanation on how to perform the multiplication using Array Multiplier.	*CO1*	*PO1*	**10**
			UNIT - V			
	9	a)	Given the instruction Load R6, 1000(R9) in the Instruction Register with R6 containing value 4200 and R9 with 85320 respectively. Show the contents of the interstage registers during the execution of the instruction using datapath in a processor. Memory location 86320 contains data 75900.	*CO2*	*PO2*	**10**
		b)	The processor generates the control signals for execution of instructions using hardware components, explain the same with a neat diagram.	*CO1*	*PO1*	**06**
		c)	Illustrate how single block memory Register File reads the content of two registers simultaneously.	*CO1*	*PO1*	**04**
			OR			
	10	a)	Write the sequence of actions needed to fetch and execute a subroutine call instruction assuming the address of the subroutine call is stored in Register R9.	*CO1*	*PO1*	**10**
		b)	Elucidate memory organization of parallel computers with distributed memory organization and shared memory organization	*CO1*	*PO1*	**10**

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