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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: CSE(DS)/AI & DS/CSE(IoT) **Duration: 3 hrs.**

Course Code: 23DC3ESCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Describe with a diagram the basic operational units present in the connection between processor and main memory. What is the role played by the processor interface in the transfer of data?	*CO1*	*PO1*	**7**
	b)	Analyze the basic operational steps involved in executing the below instructions: i) Store R5, NUM ii) Add R5, R4, R3 Outline the operation of MAR and MDR.	*CO2*	*PO2*	**7**
	c)	Perform binary addition and subtraction for operands -6 & -5. Also state the overflow condition.	*CO1*	*PO1*	**6**
		OR			
2	a)	Discuss the big-endian and little-endian byte addressing scheme with neat diagram.	*CO1*	*PO1*	**7**
	b)	Identify and explain the addressing mode used in the below instructions. i) Add R1, R2, R3 ii) Load R2, 5000(R3) iii) DIV R5, R4, #10 iv) Load R2, (R5) v) Integer X, Y, SUM vi) Branch_if_[R2]>0 Identify the data structures that can be used for organizing the data used in computations.	*CO2*	*PO2*	**7**
	c)	Write an assembly program for the following Fibonacci sequence 0, 1, 1, 2, 3, 5 and store the final result in a register	*CO1*	*PO1*	**6**

			UNIT - II			
	3	a)	Define Memory Mapped I/O. Demonstrate the process that takes place when moving a character from the keyboard to the processor and from processor to display.	*CO1*	*PO1*	**10**
		b)	Consider a scenario when two or more devices contend to access a shared resource such as a bus. Discuss the approach that could provide orderly access to the shared resource.	*CO2*	*PO2*	**10**
			OR			
	4	a)	i) Explain push and pop operation in stacks with suitable code snippet in assembly program. ii) It is often necessary to perform a particular task many times on different data values. Elaborate on how would you implement this task with suitable registers using subroutines.	*CO1*	*PO1*	**5+5**
		b)	Consider a scenario where devices D1 and D2 may request an interrupt at the same time while an interrupt caused by device D3 is being serviced. Illustrate the possible approaches to handle this situation by the processor.	*CO2*	*PO2*	**10**
			UNIT - III			
	5	a)	Explain with a neat sketch, structure of Synchronous DRAM and its timing diagram for a typical burst read of length 4.	*CO1*	*PO1*	**10**
		b)	You are a computer architect trying to design a cache memory with 128 blocks of 16 words each that can store main memory blocks. Design the different mapping strategies for determining where the memory blocks are placed in the cache.	*CO3*	*PO3*	**10**
			OR			
	6	a)	Elucidate on virtual memory. Illustrate translation of virtual address to physical address with block diagram.	*CO1*	*PO1*	**10**
		b)	A data intense application requires a direct transfer of large blocks of data at high speed between the external device and the main memory. Demonstrate the technique and registers required to achieve the task.	*CO3*	*PO3*	**10**
			UNIT - IV			
	7	a)	Design a 4-bit adder using a carry- look ahead logic and derive the generate and propagate functions. Also compare 4-bit adder with the 16-bit adder.	*CO3*	*PO3*	**10**
		b)	i) Apply sequential circuit multiplication for Multiplicand 7 and Multiplier -3.	*CO1*	*PO1*	**10**

			ii) Multiply A= 010111(+23) and B =110110(-10) using Booth's bit pair recoding multiplication method.			
			OR			
	8	a)	Design a carry save array for a 4*4 multiplier. Demonstrate with an example how Booth's bit pair recoding of multiplier can improve the speed of multiplication?	*CO3*	*PO3*	**10**
		b)	Perform restoring and non-restoring division for the given dividend and divisor A = 1001 and B = 0010	*CO1*	*PO1*	**10**
			UNIT - V			
	9	a)	Discuss the data path organization in a computer in detail with relevant diagrams.	*CO1*	*PO1*	**10**
		b)	With a neat diagram, elucidate Hardwired Control Unit organization.	*CO1*	*PO1*	**6**
		c)	Illustrate the sequence of actions needed to fetch and execute the branch instruction with an example.	*CO1*	*PO1*	**4**
			OR			
	10	a)	Elucidate the four phases in the evolution of microprocessor design, and how has the internal use of parallelism influenced each of these phases?	*CO1*	*PO1*	**10**
		b)	Outline Flynn's classification of parallel architecture.	*CO1*	*PO1*	**6**
		c)	Write a note on thread level parallelism.	*CO1*	*PO1*	**4**

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