U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Computer Science and Business Systems **Duration: 3 hrs.**

Course Code: 23BS3PCCOA **Max Marks: 100**

Course: Computer Organization & Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			CO	PO	Marks
		UNIT - I			
1	a)	Analyze the functions of the following processor registers: MAR, MDR, PC & IR.	*CO 1*	*PO2*	**10**
	b)	Illustrate with an example, the usage of stacks in a subroutine call.	*CO 1*	*PO1*	**10**
		OR			
2	a)	Examine logical and arithmetic shift and rotate instructions, with examples.	*CO 1*	*PO1*	**10**
	b)	Detail out on byte addressability and its types.	*CO 1*	*PO1*	**10**
		UNIT - II			
3	a)	Define Bus arbitration. Explain Centralized bus arbitration with a neat diagram.	*CO 2*	*PO1*	**10**
	b)	Detail out on the registers used in DMA Interface.	*CO 2*	*PO1*	**10**
		OR			
4	a)	Illustrate the different ways of enabling and disabling interrupts.	*CO 2*	*PO1*	**10**
	b)	Discuss Asynchronous bus operation. Explain the handshake control of data transfer during input operation with the detailed timing diagram.	*CO 2*	*PO1*	**10**
		UNIT - III			
5	a)	Differentiate Direct mapping and Associative mapping techniques in detail, with relevant diagrams.	*CO 3*	*PO2*	**10**
	b)	Calculate the average access time experienced by processor if miss penalty is 17 clock cycles and Miss rate is 10% and cache access time is 1 clock cycle. Assume 1 clock cycle=10ns.	*CO 3*	*PO1*	**10**

			OR			
	6	a)	With a diagram, explain the internal organization of 2M X 8 Asynchronous DRAM chip.	*CO 3*	*PO1*	**10**
		b)	A block set associative cache consists of a total of 64 blocks divided into 4 block sets. The Main Memory contains 4096 blocks each containing 128 words. a) How many bits are there in Main Memory address? b) How many bits are there in each of the TAG, SET & WORD fields	*CO 3*	*PO1*	**10**
			UNIT - IV			
	7	a)	Perform multiplication for -13 and +09 using Booth's algorithm. Show all the steps clearly.	*CO 3*	*PO1*	**10**
		b)	Detail out on IEEE standard representation for floating point numbers.	*CO 3*	*PO1*	**10**
			OR			
	8	a)	Perform restoring division for 10÷3 showing all the steps.	*CO 3*	*PO1*	**10**
		b)	Outline the addition and subtraction rules which can be applied for floating point numbers with an example.	*CO 3*	*PO1*	**10**
			UNIT - V			
	9	a)	Detail out on the Hardware components of a computer.	*CO 2*	*PO1*	**10**
		b)	Examine the Processor Architecture and Technology Trends in brief.	*CO 2*	*PO1*	**10**
			OR			
	10	a)	Differentiate different types of Flynn's Taxonomy of Parallel Architectures.	*CO 2*	*PO2*	**10**
		b)	Explain in detail about Thread-Level Parallelism.	*CO 2*	*PO1*	**10**

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