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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Computer Science and Business Systems **Duration: 3 hrs.**

Course Code: 23BS3PCCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			UNIT - I	***CO***	***PO***	**Marks**
1	a)		Mention the special purpose registers inside the CPU. With a neat diagram, discuss how CPU and memory interact in executing an instruction.	***CO1***	***PO 1***	**10**
	b)		Convert the following pair of decimal number to 5 bit signed 2's complement binary number and perform addition. State whether overflow occurs or not in each case. i) −10 and +3 ii) +14 and −12 iii) +13 and +11 iv) − 9 and +14 v) −12 and +9	***CO1***	***PO1***	**10**
			OR			
2	a)		Define Addressing modes. Register R1 and R2 contain values 1800 and 3800 respectively. The word length of the processor is 4 bytes. What is the effective address of the memory operand in each one of the following cases? i. ADD 100 (R2), R6. ii. LOAD R6, 20 (R1, R2) iii. STORE –(R2), R6 iv. SUBTRACT (R2) +, R6 v. MOV #3, R4	***CO1***	***PO1***	**6**
	b)		Provide an Assembly language program to add n numbers with the use of indirect addressing mode.	***CO1***	***PO1***	**8**
	c)		Define byte addressability. With an example, explain two different types of byte addressability.	***CO1***	***PO1***	**6**
			UNIT - II			
3	a)		What is the purpose of stack pointer and frame pointer? With an example, explain the working of stack frames for nested subroutines.	***CO1***	***PO1***	**10**

		b)	Few applications require the bits of an operand to be shifted right or left some specified number of bit positions. Detail out with an example, shift and rotate instructions for general binary coded information.	***CO1***	***PO1***	**10**
			OR			
	4	a)	What is Program controlled I/O. With a neat diagram, explain the mechanism used to synchronize the transfer of data between processor and I/O devices along with the registers used in the keyboard and display interfaces.	***CO1***	***PO1***	**10**
		b)	Number of devices capable of initiating interrupts are connected to the processor. Devices are operationally independent, there is no definite order in which they will generate interrupts. Considering the situation, justify the following: i. How can the processor determine which device is requesting an interrupt? ii. Given that different devices are likely to require different interrupt-service routines; how can the processor obtain the starting address of the appropriate routine in each case? iii. Should a device be allowed to interrupt the processor while another interrupt is being serviced?	***CO1***	***PO2***	**10**
			UNIT - III			
	5	a)	With a neat diagram, explain the internal organization of a 16 x 8 memory chip. Specify in detail the number of external connections required.	***CO3***	***PO1***	**10**
		b)	Interpret the significance of Direct Memory Access(DMA) approach and the registers used in a DMA interface.	***CO3***	***PO1***	**10**
			OR			
	6	a)	With respect to speed, cost and size, examine the hierarchy of memory.	***CO3***	***PO1***	**6**
		b)	Compare direct and associative mapping functions relevant to cache memories with appropriate illustrations.	***CO3***	***PO2***	**8**
		c)	With a neat diagram, explain the typical organization that implements virtual memory.	***CO3***	***PO1***	**6**
			UNIT - IV			
	7	a)	Detail out the general organization and working of a 4-bit carry look ahead adder with a neat diagram.	***CO3***	***PO1***	**10**
		b)	With a neat diagram, explain the working of a sequential circuit binary multiplier. Perform (-13) x (+11) using sequential multiplication.	***CO3***	***PO1***	**10**
			OR			
	8	a)	Perform multiplication for the given signed numbers using Booth's algorithm and Fast-Bit pair recoding method: Multiplicand: – 11 and Multiplier: +27	***CO3***	***PO1***	**10**

		b)	Write the steps for performing non-restoring division algorithm. Perform 8 divide 3 using non-restoring division technique.	***CO3***	***PO1***	**10**
			UNIT - V			
	9	a)	With an example, illustrate the sequence of actions needed to fetch and execute an unconditional branch instruction.	***CO2***	***PO1***	**10**
		b)	Discuss the four categories of Flynn's taxonomy for parallel architectures.	***CO2***	***PO1***	**10**
			OR			
	10	a)	With a neat diagram, detail out the working of control signal generation using hardwired control technique.	***CO2***	***PO1***	**10**
		b)	Distinguish the three different types of architectures of a multicore processors with an example.	***CO2***	***PO1***	**10**

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