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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

August 2024 Supplementary Examinations

Program: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 19CS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

SUPPLEMENTARY EXAMS 2024

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Define Addressing Mode. Explain all the Addressing Modes with example.	CO1	PO1	10
	b)	Convert the following pairs of decimal numbers to 5-bit 2's-complement numbers, then add them. State whether or not overflow occurs in each case: a. 5 and 10 b. 7 and 13 c. -14 and 11 d. -5 and 7	CO1	PO2	10
		UNIT - II			
2	a)	How can the processor recognize the device requesting an interrupt? Given that different devices are likely to require different interrupt-service routines, how can the processor obtain the starting address of the appropriate routine in each case? Should a device be allowed to interrupt the processor while another interrupt is being serviced? How should two or more simultaneous interrupt request be handled?	CO2	PO2	10
	b)	Suppose that two decimal digits represented in ASCII code are located in the memory at byte locations LOC and LOC + 1. We wish to represent each of these digits in the 4-bit BCD code and store both of them in a single byte location PACKED. The result is said to be in *packed-BCD* format. Write sequence of instructions for this task. Also indicate the memory location values with their ASCII codes.	CO2	PO2	10
		OR			
3	a)	Explain Synchronous Data Transfer or Synchronous Bus. Also explain the timing diagram of an input transfer on a synchronous bus.	CO2	PO2	10
	b)	Analyze Interrupt Driven Input/ Output data transfer with the program indicating interrupt service routine. Also indicate the keyboard interface, display interface and control registers used.	CO2	PO2	10

			UNIT - III			
	4	a)	Analyze the working of DMA controller with a neat diagram. Also explain Direct Memory Access operation indicating the status and control bits.	***CO3***	***PO3***	**10**
		b)	Design and explain a memory of size 8M x 32 using 512K x 8 memory chips.	***CO3***	***PO3***	**10**
			OR			
	5	a)	Explain Direct-mapped cache with an example. A cache is organized in the direct-mapped manner with the following parameters: Main memory size 128K words Cache size 2K words Block size 256 words i. How many bits are there in a main memory address? ii. How many bits are there in each of the TAG, BLOCK and WORD fields? Write the main memory address diagram indicating the above 3 fields	***CO3***	***PO3***	**10**
		b)	Analyze with a neat diagram, the use of an Associative-mapped translation lookaside buffer in Virtual memory.	***CO3***	***PO2***	**10**
			UNIT - IV			
	6	a)	Assuming 6-bit 2's-complement number representation, multiply the multiplicand A = -23 by the multiplier B = 16 using the Bit-Pair Recoding algorithm. Show the solving steps completely and clearly.	***CO3***	***PO3***	**10**
		b)	Using non-restoring division algorithm, divide 8 by 3. Show by solving steps completely and clearly.	***CO3***	***PO3***	**10**
			UNIT - V			
	7	a)	Considering five-stage Datapath in a processor, write Sequence of actions needed to fetch and execute each of the following instructions: i. Subtract R1, R2, R3 ii. Store R4, X(R5) iii. Conditional branch instruction Branch_if_[R6]>=[R7] LOOP	***CO3***	***PO3***	**10**
		b)	Explain Flynn's Taxonomy Classification according to important characteristics of a parallel computer with neat diagrams	***CO3***	***PO2***	**10**

SUPPLEMENTARY EXAMS 2024

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