U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science And Engineering **Duration: 3 hrs.**
Course Code: 19CS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture **Date: 21.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may suitably assumed.

UNIT - I

1 a) Convert the following pairs of decimal numbers to **6-bit** Two's-complement numbers, then subtract them, where the second number of each pair is to be subtracted from the first number. State whether or not overflow occurs in each case **8**

i. 15 and 13
ii. -20 and -31
iii. -14 and 11
iv. -10 and -13

b) Write assembly level language program to find sum of Test marks. Consider the data arrangement as follows in the memory location. **8**

Memory label	Each location four bytes
N	Number of Students
List	Student-ID-1
List+4	Test-1
	Test-2
	Student-ID-2
	Test-1
	Test-2
	Student-ID-3
	…….
Sum-Test-1	
Sum-Test-2	

c) Explain Big-endian and Little-endian memory byte addressing schemes with an example. **4**

UNIT - II

2	a)	Suppose that four ASCII characters are contained in the 32-bit register R2. In some task, we wish to determine if the rightmost character is **A**. If it is, then a conditional branch to FOUNDA is to be made. Write sequence of instructions for this task. Note: Assume the hexadecimal ASCII value for the character **A** is 0x41	**5**
	b)	Discuss the concept of Bus Arbitration with a neat diagram.	**5**
	c)	For the task of adding N numbers, write an assembly language program to demonstrate passing of parameters to Subroutine using stack	**10**

OR

3	a)	Differentiate between Logical right shift and Logical left shift instruction with example for each.	**5**
	b)	Considering Interrupt Driven Input-Output data transfer, explain the concept of "Vectored Interrupts"	**5**
	c)	Demonstrate with neat timing diagrams the Asynchronous Bus operation for Input and Output data transfer and explain.	**10**

UNIT - III

4	a)	With neat diagram show the design of internal organization of a 32Mx8 dynamic memory chip and explain.	**10**
	b)	Describe the Read only Memory and discuss different types of ROMs used	**5**
	c)	With neat diagram explain Memory Hierarchy	**5**

OR

5	a)	Design a Memory of Size 16Mx32 using 1024Kx8 memory chips. Show the design with neat and complete diagram. Specify the number of address lines.	**10**
	b)	A cache is organized in the direct-mapped manner with the following parameters: Main memory size 64K words Cache size 2K words Block size 16 words i. How many bits are there in a main memory address ? ii. How many bits are there in each of the TAG, BLOCK and WORD fields ?	**5**
	c)	Analyze and illustrate the process of translating Virtual Memory Address to physical address with a neat diagram.	**5**

UNIT - IV

6	a)	Assuming 6-bit Two's-complement number representation, multiply the following numbers using the Booth Bit-Pair Recoding algorithm i. Multiplicand A = -13 Multiplier B = -20 ii. Multiplicand A = 23 Multiplier B = -10	**8**

	b)	Demonstrate the division of 25 by 4 using restoring division algorithm.	**6**
	c)	Represent the number -307.1875 in IEEE single and double precision floating point number formats.	**6**

UNIT - V

7	a)	According to Flynn's taxonomy, list and explain different classifications of Parallel computers.	**8**
	b)	With neat block diagram explain Hardwired control unit	**8**
	c)	Considering five-stage organization of Data path in a processor, write Sequence of actions needed to Fetch and execute the instruction Load R5, X(R7)	**4**

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