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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 22CS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture **Date: 08.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

B.M.S.C.E.- ODD SEM 2022-23

UNIT - I

1 a) Convert the following pairs of decimal numbers to 5-bit 2's complement numbers, and then perform addition and subtraction on each pair. Indicate whether or not overflow occurs for each case. **10**
(i) 7 and 13 (ii) -12 and 9.

b) With a neat diagram explain functional units of a computer. **05**

c) Define Addressing Mode. Explain any four Addressing Modes with example. **05**

UNIT - II

2 a) With respect to interrupts explain **10**
i. Polling
ii. Vectored interrupt
iii. Interrupt Nesting

b) Explain the concept of parameter passing by value and reference with a program of adding two numbers. **10**

UNIT - III

3 a) Demonstrate the translation of Virtual Address to Physical Address with a neat diagram. **10**

b) i. With necessary diagram design and explain organization of 1Kx1 memory chip. Arrange the memory cells in the form rows and columns with necessary decoder and multiplexer. **10**
ii. Suppose cache memory has 128 blocks and main memory has 4K blocks. Each block consists of 16 words. Each word size is of one byte. Determine number of tag bits, set bits and block bits in case of Set associative mapping with each set comprising of 2 blocks.

OR

4 a) Explain the different cache mapping techniques. **10**

b) **i.** Design 4M x 16 memory using 512K x 8 memory modules. **10**

ii. A computer system uses 16-bit memory addresses. It has a 4K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

UNIT - IV

5 a) Represent $(0.0625)_{10}$ in IEEE Single Precision and Double Precision Floating point number Formats. **05**

b) Multiply the multiplicand (+22) by Multiplier (-6) using normal Booth's Multiplication method. **05**

c) Multiply 110101 (Multiplicand) by 011011 (Multiplier) using Booth's Bit-Pair Recoding Method. **05**

d) Multiply 14(Multiplicand) by 12(Multiplier) using Add-Shift Method. **05**

OR

6 a) Divide 8 by 3 using Non-Restoring Division Algorithms. **05**

b) Multiply +23(Multiplicand) by -9(Multiplier) using normal Booth's Multiplication Method. **05**

c) Multiply 010101 (Multiplicand) x 111011 (Multiplier) using Booth's Bit-Pair Recoding Method. **05**

d) Represent $(-314.63)_{10}$ in IEEE Single Precision and Double Precision Floating point number Formats. **05**

UNIT - V

7 a) Describe the taxonomy of FLYNN's in parallel architecture. **10**

b) Explain with block diagram the basic organization of a Hardwired Control Unit. **10**

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