

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2023 Supplementary Examinations

Programme: B.E.

Branch: Computer Science and Engineering

Course Code: 22CS3PCCOA

Course: Computer Organization and architecture

Semester: III

Duration: 3 hrs.

Max Marks: 100

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

- 1 a) Explain basic operational concepts with diagram showing the connection between Processor and Memory. **10**
- b) Define Addressing mode. List any five addressing modes and explain with suitable examples. **10**

UNIT - II

- 2 a) Explain Stack Frame. **5**
- b) With necessary diagram explain input operation in handshake mode. **5**
- c) Write an assembly language program to read a line of text and print it using program controlled I/O. **10**

UNIT - III

- 3 a) With neat diagram explain internal organization of 1Kx1 memory chip with necessary decoder and multiplexer. **10**
- b) Explain different Cache mapping techniques. **10**

OR

- 4 a) List different types of Read Only Memories (ROM) and explain. **6**
- b) Explain static RAM cell with neat diagram. **4**
- c) Design a memory of size 2Mx32 using 512Kx8 Memory chips. Show the design with neat and complete diagram. **10**

UNIT - IV

- 5 a) Apply normal Booth multiplication algorithm and solve **10**
 - (i) 13(multiplicand) and -6 (multiplier)
 - (ii) 23 (multiplicand) and -9 (multiplier)
- b) Perform division operation using Restoring methods for the following **10**
 - (i) Dividend (8) = (1000) Divisor (3) = (0011)

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

OR

- 6 a) Apply Booth Bit-pair recording algorithm and multiply the following: **10**
i. -13(Multiplicand) and -20 (Multiplier)
ii. +23 (Multiplicand) and -10 (Multiplier)
- b) Design and describe the working of a 4-bit carry look-ahead adder **10**

UNIT - V

- 7 a) Considering five-stage datapath in a processor, write sequence of actions needed to fetch and execute the following instructions **10**
i. Add R3, R2, R1
ii. Store R6, X(R8)
- b) Discuss the operation of hardwired control unit with suitable diagram **10**
