U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 22CS3PCCOA **Max Marks: 100**
Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	With a neat diagram explain basic operational concepts between memory & processor. Considering this diagram, list the steps needed to execute the instruction Add (R1) +, R0	CO1	PO1	**10**
	b)	Write assembly language program to add contents of an array. Consider the number of elements of the array is stored starting at the memory location N and array elements are stored starting at memory location NUM I . For writing assembly language program you can consider using combination of both instruction formats i.e., two — addresss format of "OPCode SourceOperand DestinationOperand" or "One-address format of OPCodc Operand".	CO2	PO1	**10**
		UNIT - II			
2	a)	Suppose distributed bus arbitration is used for connecting various devices. Apply this technique to resolve the situation "if devices with numbers 3 and 6 are competing "Which device will emerge as winner and how?	CO2	PO1	**08**
	b)	With necessary diagram explain daisy chain arrangement used for connecting multiple devices.	CO2	PO1	**06**
	c)	With a neat diagram explain the centralized bus arbitration technique.	CO2	PO1	**06**
		UNIT - III			
3	a)	Design 4Mx16 memory module using 512K x 8 static memory chips. Show your design with neat diagram.	CO3	PO2	**10**
	b)	List and explain three different mapping techniques used in cache Memories with an example.	CO3	PO2	**10**
		OR			
4	a)	Design a memory chip of size l K x 1. Arrange the memory cells as a matrix of32-bits x 32-bits. Show your design with neat diagram.	CO3	PO2	**10**

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		b)	Suppose that in a computer a cache with 8-word blocks is used. Assume it takes 1 clock cycle to send address to main memory. The main memory is DRAM. To fetch the first word 8 clock cycles are required, but the subsequent words of the block are accessed in 4 clock cycles per word. If a single memory module is used, calculate the number of clock cycles (or time) needed to load the desired block into cache? Suppose that memory is constructed as four modules using interleaved technique with consecutive words in consecutive modules. Now calculate the number of clock cycles (or time) needed to load the desired block into cache?	*CO3*	*PO2*	**10**
			UNIT - IV			
	5	a)	Multiply 010111(Mu1tiplicand) and 110110(Multiplier) using bit pair recoding algorithm.	*CO3*	*PO2*	**05**
		b)	Convert I2.890625 to IEEE 32bit and 64-bit floating-point format.	*CO3*	*PO2*	**10**
		c)	Multiply (-11) x (+27) using booths Algorithm.	*CO3*	*PO2*	**05**
			OR			
	6	a)	Add 12.68 and 23.26 using floating point addition.	*CO3*	*PO2*	**05**
		b)	Multiply 13 x 11 using sequential binary multiplier.	*CO3*	*PO2*	**05**
		c)	Perform 8/3 using Restoring & non-restoring Algorithm.	*CO3*	*PO2*	**10**
			UNIT - V			
	7	a)	List and explain different classifications of parallel completer according Flynn's Taxonomy.	*CO3*	*PO2*	**10**
		b)	Explain the Hardwired control unit with a neat diagram.	*CO3*	*PO2*	**10**

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