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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## August 2023 Semester End Make-Up Examinations

**Programme: B.E.** **Semester: III**
**Branch: Computer Science and Engineering** **Duration: 3 hrs.**
**Course Code: 22CS3PCCOA** **Max Marks: 100**
**Course: Computer Organization and Architecture** **Date: 14.08.2023**

**Instructions**: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

### UNIT - I

1 a) Explain basic operational concepts with diagram showing the connection between Processor and Memory. **6**

b) Describe Register Indirect and Base with Index addressing modes with an example. **4**

c) Convert the following pairs of decimal numbers to **6-bit** Two's-complement numbers, then add them. State whether or not overflow occurs in each case **10**
i. 15 and 13
ii. -20 and -31
iii. 7 and -13
iv. -12 and 9

### UNIT - II

2 a) With neat timing diagram explain input data transfer of a Synchronous bus. **6**

b) Describe Bus Arbitration with neat diagram. **4**

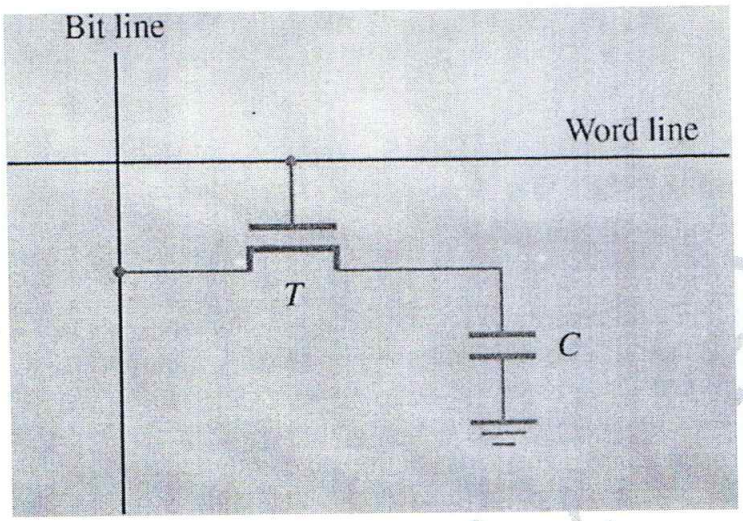
c) Write an assembly level language program to add n numbers using subroutine. Consider the memory location where the label **N** contains n value, list of n numbers is stored starting from the memory location with label the **NUMBER** and sum of n numbers should be stored at memory location with label **TOTAL**. Use the stack to pass the parameters **N** and **NUMBER** from main program to subroutine and return sum. **10**

**Note:**
i. If required inside subroutine you can use stack to save the register contents which are used inside the subroutine.
ii. Can pass the parameters using either pass by value or pass by reference.
iii. Consider each memory location capacity as four bytes.

### UNIT - III

3 a) Consider the dynamic memory cell as shown in the below Figure. Assume that C = 50 femtofarads ($10^{-15}$ F) and that leakage current through the transistor is **4**

about 10 picoamperes ($10^{-12}$ A). The voltage across the capacitor when it is fully charged is 5.5V. The cell must be refreshed before this voltage drops below one volt (1V). Estimate the minimum refresh rate. Note: Show the solving steps clearly and completely.




b) A block-set-associate cache consists of a total of 128 blocks divided into 4-block sets (i.e., four blocks per set). The main memory contains 4096 blocks, each consisting of 64 words. **6**

i. How many bits are there in a main memory address ?

ii. How many bits are there in each of the TAG, SET and WORD fields ?

Note: Show the solving steps clearly and completely.

c) Design a Memory of Size 4Mx32 using 1024Kx8 memory chips. Show the design with neat and complete diagram. **10**

**OR**

4 a) List different types of Read Only Memories (ROM) and explain **6**

b) Describe Memory Hierarchy with neat diagram. **6**

c) With neat block diagram explain Virtual Memory Address Translation. **8**

**UNIT - IV**

5 a) Design a Subtractor using Full-adders to subtract two four-bit numbers. Illustrate the design with suitable diagram and expressions. **10**

b) i. Assuming 6-bit 2's-complement number representation, multiply the multiplicand A = -14 by the multiplier B = 19 using the Booth Bit-Pair Recoding algorithm **10**

ii. Repeat above problem for Multiplicand A = 15 and Multiplier B = -11

**OR**

6 a) **i.** Using restoring division algorithm, divide 25 by 4 **10**

**ii.** Using non-restoring division algorithm, divided 20 by 5

Show the solving steps completely and clearly.

b) Represent the number 0.0625 in IEEE single and double precision floating point number formats. **6**

c) Illustrate the rules needed for Add/Subtract of Floating Point numbers. **4**

## UNIT - V

7 a) Considering five-stage Datapath in a processor, write Sequence of actions needed to fetch and execute the instruction Add R1, R2, R3 **6**

b) With neat diagram show the design of Hardwired control unit and describe. **8**

c) List and explain different levels of Internal Parallelism. **6**

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