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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Computer Science and Engineering **Duration: 3 hrs.**

Course Code: 23CS3ESCOA / 22CS3PCCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Represent the decimal values 55, -31, 48, -20, 39 as signed 8-bit numbers in the following formats a. Sign-Magnitude b. 1's complement c. 2's complement	*CO2*	*PO3*	**10**
	b)	i. Convert the following pairs of decimal numbers to 8-bit 2's-complement numbers, then add them. State whether or not overflow occurs in each case: a. 81 and 52 b. -33 and -64 ii. Repeat the process for subtraction where the second number is to be subtracted from the first number. State whether or not overflow occurs in each case.]	*CO2*	*PO3*	**10**
		OR			
2	a)	i. Write the sequence of instructions to solve the given expression: P = (A + B) – C * D + (E / F) Note that A, B, C, D are names of memory locations of four bytes each. Consider general purpose registers like R1, R2, R3, etc. without changing the contents of A, B, C, D, E, F. ii. Analyze the byte-addressable memory contents for the hexadecimal number 0x2739361734290548. Indicate the 32-bit words with the contents in Little– endian and Big-endian scheme. Note that the two memory words are stored at locations 5040 and 5044	*CO2*	*PO3*	**10**
	b)	Define Addressing Mode. Explain any 5 Addressing modes with an example.	*CO1*	*PO1*	**10**
		UNIT - II			
3	a)	Write an assembly level language program with a subroutine STRING_CONCAT to concatenate two strings. Note that there are two strings stored in memory starting at address STR1 and	*CO3*	*PO3*	**10**

			STR2 respectively. The string ends with the carriage return (CR) character with ASCII code 0x0D. Write an assembly level language program to store the concatenated strings in a memory starting at address RESULT.			
	3	b)	Explain in detail about Stack Frame with a neat diagram.	*CO3*	*PO3*	**10**
			OR			
	4	a)	Write RISC-style program that reads a line of characters and displays it.	*CO2*	*PO1*	**10**
		b)	Explain Shift and Rotate instructions with an example.	*CO2*	*PO1*	**10**
			UNIT - III			
	5	a)	Explain Synchronous DRAMs with neat diagram.	*CO3*	*PO1*	**10**
		b)	Design 4M x 32 memory using 512K x 32 memory modules.	*CO3*	*PO3*	**10**
			OR			
	6	a)	Explain the concept of memory hierarchy with a neat diagram.	*CO3*	*PO1*	**10**
		b)	Demonstrate Virtual Memory address translation to Physical Address with neat diagram	*CO3*	*PO1*	**10**
			UNIT - IV			
	7	a)	i. Multiply 1101(Multiplicand) and 1011(Multiplier) using ADD-SHIFT Method. Show the solving steps completely and clearly. ii. Assuming 5-bit 2's-complement number representation, multiply the multiplicand A = 13 by the multiplier B = -6 using the Booth Multiplication algorithm. Show the solving steps completely and clearly.	*CO3*	*PO3*	**10**
		b)	Multiply 45 and 63 using Carry Save Addition Method. Show the solving steps completely and clearly.	*CO3*	*PO3*	**10**
			OR			
	8	a)	Using restoring and non-restoring division algorithm, divide 1000 by 11. Show the solving steps completely and clearly.	CO3	PO3	10
		b)	Assuming 6-bit 2's-complement number representation, multiply the multiplicand A = -23 by the multiplier B = 16 using the Bit Pair Recoding algorithm. Show the solving steps completely and clearly.	CO3	PO3	10
			UNIT - V			
	9	a)	Considering five-stage Datapath in a processor, write Sequence of actions needed to fetch and execute each of the following instructions: i. Load R5, X(R7) **ii.** Unconditional branch instruction **iii**. Call Register R9	*CO3*	*PO3*	**10**

		b)	Analyze basic block organization of a hardwired control unit with diagram	*CO3*	*PO3*	**10**
			OR			
	10	a)	Differentiate between an UMA multi-processor and NUMA multiprocessor	*CO2*	*PO1*	**05**
		b)	Illustrate the two methods that can be used to resolve the cache coherence.	*CO3*	*PO2*	**05**
		c)	Explain two alternatives for implementing dual port register file, with neat diagram.	*CO3*	*PO1*	**10**

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