U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 23CS3ESCOA **Max Marks: 100**
Course: Computer Organization & Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Represent 65 and -85 using sign magnitude, 1's complement and 2's complement representation. Use 8-bit representation.	CO1	PO 1	**6**
	b)	With a neat diagram explain basic functional units of a computer	CO1	PO1	**6**
	c)	Define addressing modes. Explain any six addressing modes with examples.	CO1	PO1	**8**
		UNIT - II			
2	a)	Define assembler directives. Explain any five assembler directives with examples.	*CO1*	*PO1*	**6**
	b)	Design an assembly language program to find sum of N numbers starting at NUM1 and store result in SUM.	*CO3*	*PO3*	**6**
	c)	Define interrupt. List the sequence of events that occur when an interrupt comes from a device.	*CO1*	*PO1*	**8**
		UNIT - III			
3	a)	With a neat diagram explain memory hierarchy used in computer.	*CO1*	*PO1*	**6**
	b)	With a neat diagram, explain how virtual memory address is converted into physical address.	*CO1*	*PO1*	**6**
	c)	With neat diagram explain direct memory mapping technique used to map main memory to cache memory. Assume main memory of 128KB, cache of 16KB and block size of 256 bytes. Memory is byte addressable. Apply direct mapping to find number of tag bits, block bits and word bits.	*CO3*	*PO3*	**8**
		OR			
4	a)	With a neat diagram explain working of a SRAM cell.	*CO1*	*PO1*	**6**
	b)	With a neat diagram explain typical organization of 1K x 1 memory chip.	*CO1*	*PO1*	**6**

		c)	Design 2M x16 memory module using 512K x 8 memory modules.	*CO3*	*PO3*	**8**
			UNIT - IV			
	5	a)	Multiply 23 (Multiplicand) and -10 (Multiplier) using Bit pair recoding technique.	*CO1*	*PO1*	**6**
		b)	Design 4-bit Ripple Carry Adder (RCA) using full adders. Calculate the number of gate delays for Sum and Carry signal generation. Show the design with neat and complete diagram.	*CO3*	*PO3*	**8**
		c)	Explain with neat diagram Single precision and double precision representation of floating-point numbers with an example.	*CO1*	*PO1*	**6**
			OR			
	6	a)	Multiply 23 (Multiplicand) and -10 (Multiplier) using Booth's multiplication.	*CO1*	*PO1*	**6**
		b)	Write algorithm for non-restoring division algorithm and explain the same with an example.	*CO1*	*PO1*	**6**
		c)	Design 4-bit carry lookahead adder. Calculate the number of gate delays for Sum and Carry signal generation. Show the design with neat and complete diagram.	*CO3, 2*	*PO3, 2*	**8**
			UNIT - V			
	7	a)	With a neat diagram explain NUMA architecture in shared memory multiprocessor systems.	*CO1*	*PO1*	**6**
		b)	Write Sequence of actions needed to fetch and execute the instruction: Add R3, R4, R5.	*CO1*	*PO1*	**6**
		c)	With a neat diagram explain hardwired control unit design.	*CO1*	*PO1*	**8**

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