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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Computer Science and Engineering **Duration: 3 hrs.**

Course Code: 23CS3ESCOA / 22CS3PCCOA / 19CS3PCCOA **Max Marks: 100**

Course: Computer Organization and Architecture

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	I. Convert the following pairs of decimal numbers to 5-bit 2's complement numbers, and then perform addition and subtraction on each pair. Indicate whether or not overflow occurs for each case. (i) 7 and 13 (ii) -12 and 9. II. Repeat the Problem (I) for the subtract operation, where the second number of each pair is to be subtracted from the first number. State whether or not overflow occurs in each case.	*CO1*	*PO2*	**10**
	b)	With neat diagram explain the Basic Functional units of a Computer.	*CO1*	*PO1*	**5**
	c)	Write a CISC-style program for computing the dot product of two vectors.	*CO1*	*PO2*	**5**
		OR			
2	a)	Define Addressing Mode. Explain any 5 addressing modes with an example.	*CO1*	*PO1*	**10**
	b)	i. Consider a computer has a byte-addressable memory organized in 32-bit words according to the Little-endian scheme. Show the contents of the two memory words at locations 2000 and 2004 after the hexadecimal number 0x8038020611121720 has been entered. ii. Repeat the problem (i) for Big-endian scheme. Note: 0x represents Hexadecimal number.	*CO1*	*PO2*	**5**
	c)	Write a sequence of instructions for the following mathematical expression X= (A+B) /E * (C*D)-F.	*CO1*	*PO2*	**5**
		UNIT - II			
3	a)	Explain the concept of parameter passing by value & reference with a program of adding two numbers.	*CO1*	*PO1*	**10**
	b)	How can the processor recognize the device requesting an interrupt? Given that different devices are likely to require different interrupt-	*CO1*	*PO2*	**10**

			service routines, how can the processor obtain the starting address of the appropriate routine in each case? Should a device be allowed to interrupt the processor while another interrupt is being serviced? How should two or more simultaneous interrupt request be handled?			
			OR			
	4	a)	Analyze the role of subroutine linkage register & stack in execution of subroutines.	*CO1*	*PO1*	**10**
		b)	Write a assembly program that finds the number of negative integers in a list of n integers and stores the count in location NEGNUM. The value n is stored in memory location N, and the first integer in the list is stored in location NUMBERS. Include the necessary assembler directives and a sample list that contains six numbers, some of which are negative.	*CO3*	*PO3*	**10**
			UNIT - III			
	5	a)	Demonstrate the Translation of Virtual Address to Physical Address with a neat diagram	*CO3*	*PO3*	**10**
		b)	With a necessary diagram design and explain organization of 1K x 1 memory chip. Arrange the memory cells in the form rows and columns with necessary decoder and multiplexer.	*CO3*	*PO3*	**5**
		c)	Suppose cache memory has 128 blocks and main memory has 4K blocks. Each block consists of 16 words. Each word size is of one byte. Determine number of tag bits, set bits and block bits in case of set associative mapping with each set comprising of 2 blocks.	*CO3*	*PO3*	**5**
			OR			
	6	a)	Explain the different cache mapping functions.	*CO1*	*PO1*	**10**
		b)	A computer system uses 16-bit memory addresses. It has a 4K-byte cache organized in a direct mapped manner with 64 bytes/ cache block. Assume that the size of each memory word is 1 byte. Calculate the number of bits in each of the TAG, BLOCK and WORD fields of the memory addresses.	*CO3*	*PO3*	**5**
		c)	Explain the concept of memory hierarchy with a neat diagram.	*CO1*	*PO1*	**5**
			UNIT - IV			
	7	a)	Explain the IEEE Floating Point Formats, Represent $(0.0625)_{10}$ in Single Precision and Double Precision Floating Point Formats.	*CO1*	*PO1*	**8**
		b)	Multiply (+22) (Multiplicand) x Multiplier (-6) using Booth's Algorithm Method. Show the solving steps completely and clearly.	*CO3*	*PO3*	**6**
		c)	Multiply 110101 (Multiplicand) x 011011 (Multiplier) using Bit-Pair Recoding Method. Show the solving steps completely and clearly.	*CO3*	*PO3*	**6**

			OR			
	8	a)	Multiply 14 x 12 using sequential circuit binary multiplier along with the hardware.	*CO3*	*PO3*	**8**
		b)	Perform 8 / 3 Division using Restoring and Non-Restoring Algorithm. Show the steps completely and clearly.	*CO3*	*PO3*	**12**
			UNIT - V			
	9	a)	Explain the sequence of actions needed to to fetch and execute the instructions. (i) Add R3, R4, R5 (ii) Load R5, X(R7) (iii) Store R6, X(R8)	*CO2*	*PO3*	**10**
		b)	With a neat diagram explain the Hardwired control unit.	*CO1*	*PO2*	**10**
			OR			
	10	a)	List the two methods to resolve Cache Coherence problem and explain.	*CO1*	*PO2*	**5**
		b)	Differentiate between UMA & NUMA multiprocessors.	*CO1*	*PO2*	**5**
		c)	Considering five-stage Datapath in a processor, write Sequence of actions needed to fetch and execute each of the following instructions: (a) Unconditional branch instruction (b) Call Register R9	*CO2*	*PO3*	**10**

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