U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science And Engineering **Duration: 3 hrs.**
Course Code: 19CS3PCLOD **Max Marks: 100**
Course: Logic Design **Date: 13.09.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may suitably assumed.

UNIT - I

1 a) Draw the K-Map for the Boolean expression below and simplify to obtain the minimal sum (SOP) and minimal product (POS): **8**
$F(a,b,c,d) = \Sigma\, m(1,2,8,9,10,12,13,14)$
Also draw the logic diagrams for the simplified expressions.

b) Given the following Boolean expression: **6**
$Y(a,b,c,d) = \Sigma\, m(0,1,2,3,10,11,12,13,14,15)$
Show the simplified NAND-NAND and simplified NOR-NOR circuit.

c) Analyze the 3-variable K-map given below and check if a hazard exists and draw the equivalent hazard-free circuit as well as the corresponding grouping in the K-map. Also, identify the type of hazard. **6**

	C'	C
A'B'	1	1
A'B	0	0
AB	1	0
AB’	1	0

OR

2 a) Prove that $A(A'+C)(A'B+C)(A'BC+C') = 0$ **4**

b) Design a circuit to output the cube of a two bit number, assuming both complement and un-complemented inputs are available. **6**

c) Minimize the Boolean function using tabular Quine McClusky method: **10**
$F(a,b,c,d) = \Sigma\, m(1,2,3,6,8,9,10,12,13,14)$

UNIT - II

3 a) Analyze the working of 4-to-1 multiplexer and use it to realize a 16-to-1 multiplexer. Represent the realization diagrammatically. **6**

b) Design a logic circuit that realizes following three functions using a 3*4*2 PLA: **8**
$F1(x,y,z) = \Sigma\, m(0,1,3,5)$
$F2(x,y,z) = \Sigma\, m(3,5,7)$

c) Illustrate and explain how two 8-bit numbers can be compared using two 4-bit comparators(IC 7485). **6**

UNIT - III

4 a) With the help of logic diagram and truth table, show the working of a Master-Slave JK flip-flop. **8**

b) Starting from the basic truth table representation, illustrate how one can represent JK flip-flop, D flip-flop and T flip-flop using Characteristic equations, Finite state machines and Excitation tables. **12**

OR

5 a) With the help of logic diagram and truth table, show the working of a positive-edge-triggered RS flip-flop, along with timing diagram. **8**

b) Explain the working of a 4-bit negative-edge-triggered D-type Parallel-in-Parallel-out Shift Register, along with block diagram and showing all control inputs. **6**

c) Construct the circuit diagram for an 8-bit sequence detector which has to detect a fixed pattern "10011110" from incoming binary data stream. **6**

UNIT - IV

6 a) Explain with logic and timing diagrams, the working of a 4-bit synchronous up-down counter with JK flip-flops. **8**

b) Illustrate and explain how two Mod-5 synchronous counters can be used to realize a 5 x 2 (Mod-10) counter. **4**

c) Design a modulo-6 counter using JK flip-flops, which follows the sequence 000 – 001 - 010 – 011 – 100 – 101 – 000. **8**

UNIT - V

7 a) Draw the state transition diagram of sequence detector circuit that detects "1101" from input data stream using both Mealy and Moore model. **6**

b) Deduce the reduced state table for the following state table using Implication Table method. **8**

Present State	Next State		Present Output	
	X = 0	X = 1	X = 0	X = 1
a	f	d	0	1
b	c	f	1	1
c	f	b	1	1
d	e	g	1	1
e	a	d	1	1
f	g	b	0	1
g	a	d	0	1

c) For the state table given below, where A is input and x and y are output feedbacks: **6**

A \ xy	00	01	11	10
0	01	00	10	10
1	00	01	11	01

i) Show the stable states, if any
ii) Find out the potential problems in the state table.

******