U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

August 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 19CS3PCLOD **Max Marks: 100**
Course: Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

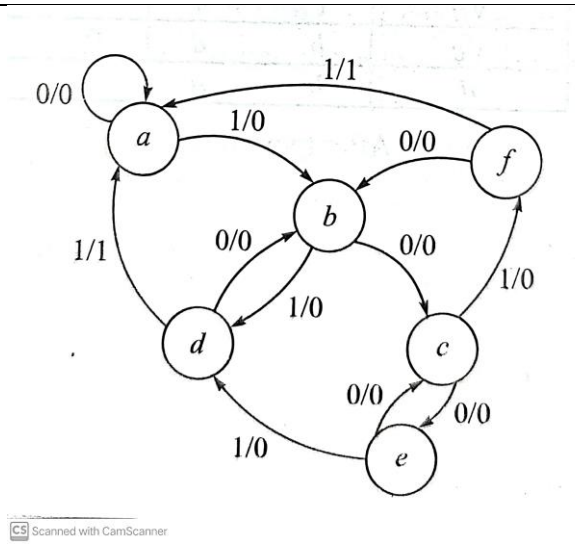
2Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	CO	PO	Marks
1	a)		Using Quine McClusky method obtain the essential prime implicants for the expression given below: $f(w,x,y,z)= \sum m(1,2,3,5,9,12,14,15) + dc(4,8,11)$	CO1	PO1	**10**
	b)		Express the following functions by minterm canonical formula and construct the corresponding truth table $f(X,Y,Z)= X'(Y'+Z) + Z'$	CO2	PO2	**05**
	c)		Analyze the following truth table. Express it in the form of SOP. Give the relevant logic diagram	CO2	PO2	**05**

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

			OR			
2	a)		Analyze the following the following scenario: There are 3 inputs x,y,z and 3 outputs a,b,c. When the binary input is 0,1,2,3 the binary output is one greater than the respective input. When binary input is 4,5,6,7 the binary output is one less than the respective binary input. Outline a truth table for this problem and design a simple circuit diagram using separate k maps for each output.	CO2	PO2	**10**
	b)		Express AND, OR and NAND using NOR gate only.	CO3	PO3	**06**
	c)		Write down all the minimal sums of the following Boolean functions using Karnaugh maps $f(a,b,c,d)= \Sigma m(3,4,6,9,11,12,13,14,15)$	CO1	PO1	**04**

			UNIT - II			
	3	a)	Design with help of truth table and k-maps 2 bit magnitude comparator	*CO3*	*PO3*	**08**
		b)	Realize each of the following Boolean expressions using a) an 8-to-1 line multiplexer where w,x,and y appear on select lines S2, S1 and S0 respectively b) an 4 to 1 mux where w and x appear on the select line $f(w,x,y,x)=\Sigma m(1,2,6,7,9,11,12,14,15)$	*CO1*	*PO1*	**08**
		c)	Design the following functions using PLA with 3 inputs, 3 product terms, 2 output. $f1(a,b,c)=\sum m(4,5,7)$ $f2(a,b,c)=\sum m(3,5,7)$	*CO1*	*PO1*	**04**
			UNIT - III			
	4	a)	With a neat diagram outline SISO - Serial IN serial Out register. Also give the timing diagram.	*CO2*	*PO2*	**06**
		b)	Derive the excitation table, characteristic equation and state transition diagram of JK and SR Flip flop.	*CO2*	*PO2*	**10**
		c)	What is bi-stable element. Illustrate how does it succeed in storing1 bit data using suitable diagram	*CO2*	*PO2*	**04**
			OR			
	5	a)	Illustrate master slave flip flop. Highlight why M.S flip flop is required.	*CO2*	*PO2*	**08**
		b)	Demonstrate the working of serial-in, parallel-out 4-bit shift register with the help of a neat diagram.	*CO2*	*PO2*	**06**
		c)	Explain the working of negative edge triggered SR flip flop with the help of a neat diagram. Also, demonstrate the timing diagram for the same.	*CO2*	*PO2*	**06**
			UNIT - IV			
	6	a)	Design 3-bit Ripple down counter. Give the timing diagram	*CO3*	*PO3*	**08**
		b)	Outline the difference between synchronous and asynchronous counter	*CO1*	*PO1*	**04**
		c)	Design a self-correcting modulo-6 synchronous counter in which all unused state leads to state CBA=000 using JK Flip-flop.	*CO3*	*PO3*	**08**
			UNIT - V			
	7	a)	Design a synchronous logic circuit using Moore model that detects a sequence 101 from an input data stream X and signals detection by making output Z=1, which otherwise is 0. Realize a circuit using JK flip flop.	*CO2*	*PO2*	**10**
		b)	What is Algorithmic state machine? List any 2 advantages of ASM.	*CO1*	*PO1*	**02**
		c)	Apply state reduction technique for the following	*CO1*	*PO1*	**08**



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