U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 19CS3PCLOD **Max Marks: 100**
Course: Logic Design

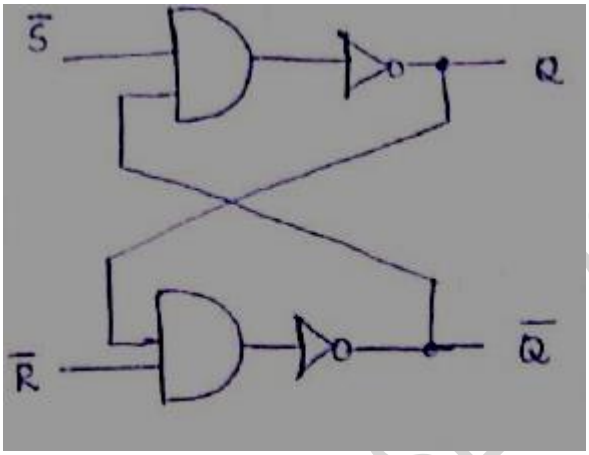
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

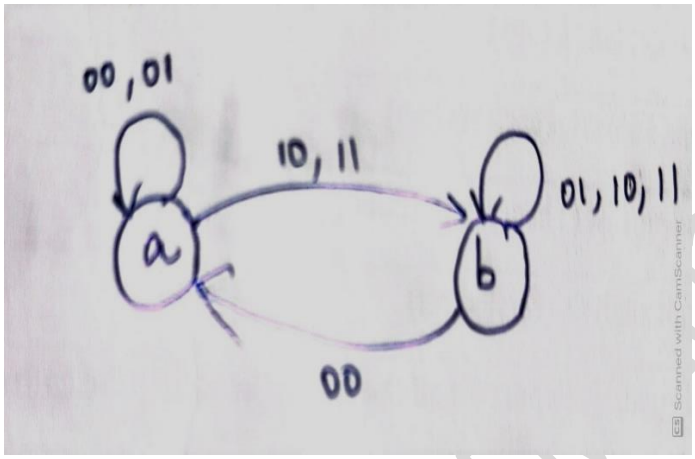
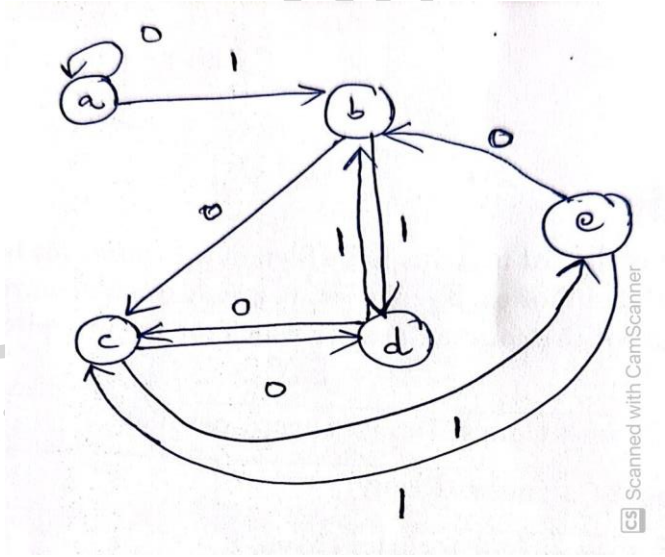
Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Draw the K-map for the Boolean expression below and simplify to obtain the minimal sum (SOP) and minimal product (POS). $f(w,x,y,z)= \sum(0,1,2,4,5,7,9,12)$ Also, draw the logic diagram for the simplified expressions.	*CO1*	*PO1*	**08**
	b)	Show the working of AND gate, NOT gate and OR gate using a NOR gate and NAND gate. Also, justify why NOR gate and NAND gate are termed as universal gates.	*CO1*	*PO1*	**06**
	c)	Analyze the 3-variable K-map given below and check if a hazard exists and draw the equivalent hazard-free circuit as well as the corresponding grouping in the K-map. Also, identify the type of hazard.	*CO2*	*PO2*	**06**

	C'	C
A'B'	0	0
A'B	1	0
AB'	1	1
AB	0	1

		OR			
2	a)	Using Quine McClusky method obtain the essential prime implicants for the expression given below: $f(w,x,y,z)= \sum(1,2,7,9,12,14,15) + dc(0,8,13)$	*CO1*	*PO1*	**10**
	b)	Simplify the expression given below using K-maps and realize the simplified expression using only NAND gates: $f(a,b,c,d) = \sum m(1,2,3,4,5,13,14) + dc(0,8,9)$	*CO1*	*PO1*	**10**
		UNIT - II			
3	a)	Realize the given 4-variable expression using 8-to-1 multiplexer as well as 4-to-1 multiplexer. $f(w,x,y,z)= \sum(0,1,3,5,9,11,15)$	*CO2*	*PO2*	**08**

		b)	Design a 3-to-8 decoder to implement the following functions: f1(x2,x1,x0)=∑m(0,2,6,7) f2(x2,x1,x0)= ∑m(3,5,6,7) Assume all the 8 output lines of the decoder are active low signals.	*CO3*	*PO3*	**06**
		c)	Design a 3*4*2 PLA for the following functions: f1(x,y,z)=∑m(0,2,4,6) f2(x,y,z)= ∑m(2,4,10)	*CO3*	*PO3*	**06**
			UNIT - III			
	4	a)	Analyze the working of the Flip flop shown below and draw the timing diagram for the same: 	*CO2*	*PO2*	**04**
		b)	List different types of Registers. Elaborate on PIPO Register using D Flip Flop.	*CO2*	*PO2*	**06**
		c)	Design a JK Flip Flop using SR Flip Flop. Represent the SR Flip Flop as well as JK Flip Flop using state transition diagram. Also, design the excitation table using the constructed state transition diagram.	*CO3*	*PO3*	**10**
			OR			
	5	a)	Explain the working of negative edge triggered SR flip flop with the help of a neat diagram. Also, demonstrate the timing diagram for the same.	*CO1*	*PO1*	**06**
		b)	Demonstrate the working of serial-in, parallel-out 4-bit shift register with the help of a neat diagram.	*CO1*	*PO1*	**06**
		c)	Design a serial adder for the addition of two 8-bit numbers using a D flip-flop.	*CO3*	*PO3*	**08**
			UNIT - IV			
	6	a)	Design a synchronous mod-6 counter using JK flip-flops for the following counting sequence: 000, 101, 001, 111, 011, 100, and then back to 000	*CO3*	*PO3*	**10**
		b)	Design a mod-8 ripple binary asynchronous down counter using JK flip flops. Clearly show the counting sequence, logic circuit as well as the timing diagram.	*CO3*	*PO3*	**10**

			UNIT - V			
	7	a)	Design a synchronous sequential circuit - Mealy model for the following problem statement: Receive the binary value 101 as input and the output becomes high (1). Also, draw the ASM chart.	*CO3*	*PO3*	**10**
		b)	Design an asynchronous sequential logic circuit for the below state transition diagram: 	*CO3*	*PO3*	**05**
		c)	Apply row elimination method to reduce the given state transition diagram: 	*CO1*	*PO1*	**05**

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