U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

Branch: Computer Science and Engineering **Duration: 3 hrs.**

Course Code: 19CS3PCLOD **Max Marks: 100**

Course: Logic Design

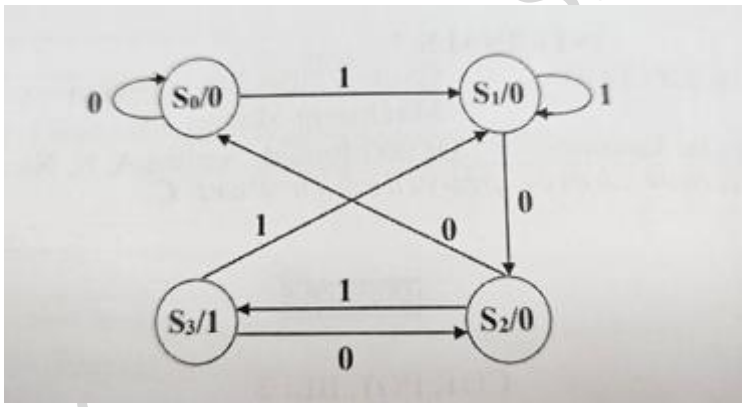
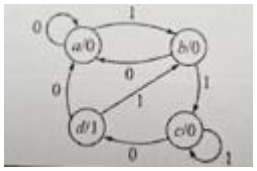
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

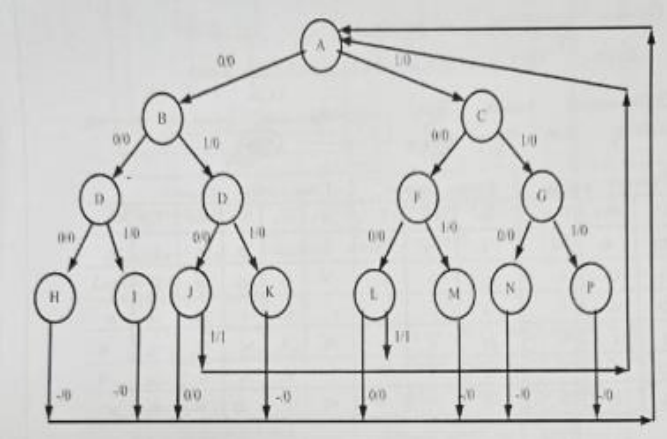
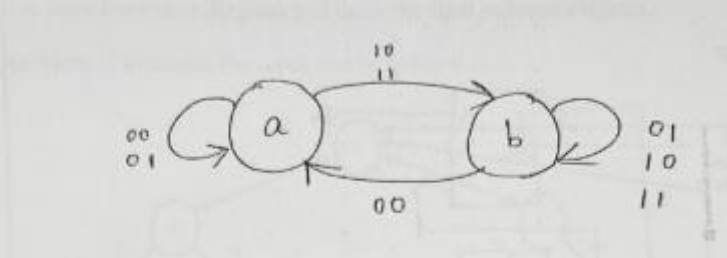
		UNIT - I	*CO*	*PO*	**Marks**
1	a)	i) Write the expression in algebraic form for the given function: $f(w,x,y,z) = \sum m(4,8,10,14)$ ii) Realize the following using only NOR gates: Y= (A+C) (B'+D')(A'+B'+C')	*CO1*	*PO 1*	**5**
	b)	Analyze the given truth table. Reduce it to SOP and draw the logic diagram.	*CO2*	*PO2*	**5**
	c)	Minimize the Boolean Function using Quine McClusky method: $f(a,b,c,d) = \sum m(0,2,3,4,8,10,12,13,14)$	*CO3*	*PO3*	**10**
		OR			
2	a)	Analyze the truth table given below for an OR gate using positive logic.	*CO2*	*PO2*	**5**

X	Y	Z	f
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

			Represent the equivalent gate using negative logic. (Here, binary 0 stands for high value and binary 1 stands for low value).			
		b)	Draw the K-map for the Boolean expression below and simplify to obtain minimal POS: f(x,y,w,z) = Πm(0,1,4,5,8,9,11)+ dc(2,10) Draw the logic diagram for the above simplified expressions.	*CO2*	*PO2*	**5**
		c)	Using Quine McCluskey method obtain the prime implicants for the expression given below: f(a,b,c,d) = ∑m(3,4,5,7,10,12,14,15) + dc(2).	*CO3*	*PO3*	**10**
			UNIT - II			
	3	a)	Design a serial adder to add 2 four-bit numbers and explain how sum and carry are generated.	*CO3*	*PO3*	**8**
		b)	Design the following functions using a 3*4*2 PLA. f1(a,b,c)= Σm(1,2,3,6) f2(a,b,c)=Σm(0,1,3,6,7)	*CO3*	*PO3*	**8**
		c)	Design a 8:1 MUX using 4:1 MUX.	*CO3*	*PO3*	**4**
			OR			
	4	a)	i) Using appropriate decoder and OR gate realize the following Boolean expression f1(a,b,c)= Σm(0,4,6) f2(a,b,c)=Σm(0,5) f3(a,b,c)=Σm(1,2,3,7) ii) With help of a truth table and circuit diagram show the design of a 1:8 De-Mux.	*CO3*	*PO3*	**10**
		b)	Using the 4 input-3 output PAL implement the functions f1(a,b,c)= Σm(0,3,5,6,7) f2(a,b,c)=Σm(1,2,3,5,7)	*CO3*	*PO3*	**10**
			UNIT - III			
	5	a)	Design a JK flip flop using SR flip flop. Represent the SR flip flop as well as JK flip flop using state transition diagram. Also, from the state transition diagram, design the excitation table.	*CO3*	*PO3*	**10**
		b)	Design a circuit diagram for an 8-bit sequence detector using one shift register and one comparator which has to detect a fixed pattern 10011110 from incoming binary data stream.	*CO3*	*PO3*	**10**
			OR			
	6	a)	A Johnson counter designed using a N-bit shift register has 2N states. When N=4, we design a switched tail-counter with 8 (clock	*CO3*	*PO3*	**10**

			pulse) states. Assume the start state as 1101. Represent the truth table and also the logic diagram for the same.			
		b)	Differentiate between the sequential circuits and combinational circuits.	*CO2*	*PO2*	**5**
		c)	Explain the SR latch debounce circuit.	*CO2*	*PO2*	**5**
			UNIT - IV			
	7	a)	Define counter. Outline the differences between synchronous counter and asynchronous counter.	*CO2*	*PO2*	**6**
		b)	Explain binary ripple counter, with its block and timing diagrams.	*CO3*	*PO3*	**8**
		c)	Write the timing diagram for 3 bit up-down counter.	*CO2*	*PO2*	**6**
			OR			
	8	a)	Design a synchronous mod-6 counter using clocked D flip flops.	*CO3*	*PO3*	**10**
		b)	Design a synchronous up counter using JK flip flop for the sequence 2,3,7,5,6,4.	*CO3*	*PO3*	**10**
			UNIT - V			
	9	a)	Explain the problem of oscillation in Asynchronous Sequential Circuit with an example. 	*CO3*	*PO3*	**5**
		b)	For the given Moore model below, illustrate the ASM chart: 	*CO2*	*PO2*	**5**
		c)	Apply State Reduction technique and eliminate the redundant states in the below state transition diagram and draw the final reduced diagram.	*CO3*	*PO3*	**10**

						
			OR			
	10	a)	Analyze the State Transition diagram given below and draw the equivalent ASM chart for the same. 	*CO2*	*PO2*	**5**
		b)	Provide the reduced state transition diagram using implication table method for the following graph:	*Co3*	*Po3*	**10**
		c)	Analyze the mealy model asynchronous sequential circuit for NAND gate. Construct the truth table for various cases.	*CO2*	*PO2*	**5**

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