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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science And Engineering **Duration: 3 hrs.**
Course Code: 19CS3PCLOD **Max Marks: 100**
Course: Logic Design **Date: 19.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may suitably assumed.

UNIT - I

1 a) Prove the following: **6**
i) x'y'z'+x'y'z+x'yz+xy'z+xyz=x'y'+z
ii)w'y'z'+wz+y'z+xyz=w'y'+wz+xz

b) Simplify and Realize the following Boolean function using NAND gates only. **6**
f(a,b,c,d)= ∑m(0, 6, 8, 9, 10, 11, 13, 14, 15)

c) Simplify the following function using K-Map in SOP and POS form. **8**
f(w,x,y,z)= ∑m(1,3,4,5,6,7,11,14,15)

OR

2 a) Using Quine McClusky method obtain the essential prime implicants for the expression given and also write the simplified expression for the same **10**
f(w,x,y,z)= ∑m(1,3,5,6,7,13,14) + dc (8,10,12)

b) Simplify the expression given below using K-maps and realize the simplified expression using basic gates: **6**
f(a,b,c,d) = ΠM (2,4,6,9,11,15) +dc(5,10,13,14)

c) What is static 0 hazard and how it can be eliminated? **4**

UNIT - II

3 a) Analyse the truth table given below for a Boolean function where A, B, C are the 3 input variables and X, Y are the output variables. Here, input A has higher priority than input B and input B has higher priority than input C. The circuit also has Enable as the input. Implement the function using basic gates. **6**

Input				Output	
Enable	**A**	**B**	**C**	**X**	**Y**
0	X	X	X	0	0
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	X	1	0
1	1	X	X	1	1

b) Realize the given 4-variable expression using 8-to-1 multiplexer as well as 4-to-1 multiplexer. **8**
f(w,x,y,z)= ∑(2,5,6,7,9,12,13,15)

c) Using OR and/or NOR gates along with 3-to-8 decoder to implement the following functions. The gates should be selected so as to minimize the number of inputs. **6**
i) f1(x,y,z)=ΠM(1,2,5)
f2(x,y,z)= ΠM (0,1,3,5,7)

ii) f1(x,y,z)= ∑m(1,3)
f2(x,y,z)= ∑m (1,2,4,5,7)

Assume all the 8 output lines of the decoder are active high signals.

UNIT - III

4 a) Explain the working of positive edge triggered JK flip flop with the help of a neat diagram. Also, demonstrate the timing diagram for the same **8**

b) Derive the characteristic equations for **8**
i) SR Flip Flop
ii) D Flip Flop
iii) JK Flip Flop
iv) T Flip Flop
Also represent all the above flip flops using state transition diagram.

c) Differentiate Ring Counter and switched tail counter. **4**

OR

5 a) Demonstrate the working of serial-in, serial-out 4-bit shift register with the help of a neat diagram. **6**

b) Design a 4 bit sequence detector using D Flip Flop to detect a pattern '1010' in the input sequence. **8**

c) With a neat diagram explain the working of SR Flip Flop realized using NAND gates. **6**

UNIT - IV

6 a) Design a 3 bit asynchronous up- down counter using JK Flip Flop. **8**

b) Design a synchronous mod-6 counter using JK flip-flops for the following counting sequence: **12**
000, 010, 011, 110, 101, 001 and then back to 000

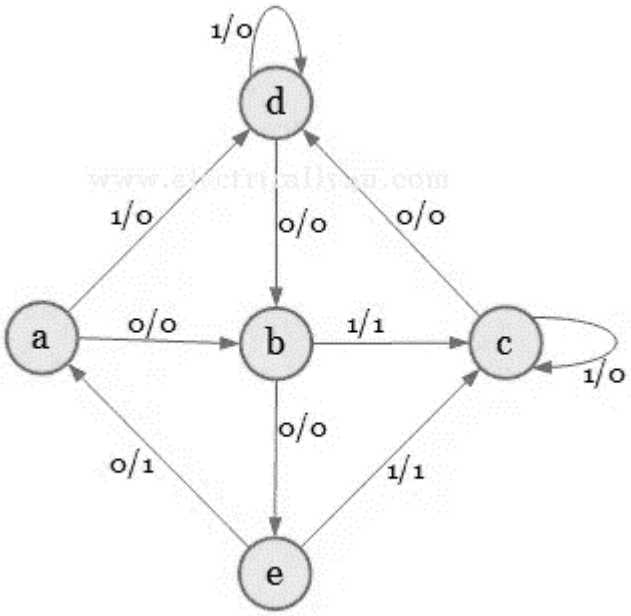
UNIT - V

7 a) Design a synchronous sequential circuit using Moore Model for the sequence detector to detect 3 or more consecutive 1's in the given sequence. **8**

b) Obtain the reduced state table for the state diagram given below using **8**

i) Row elimination method

ii) Implication table method



c) Differentiate Moore model and Mealy model. **4**

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