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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 22CS3PCLOD **Max Marks: 100**
Course: Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Draw the K-map for the Boolean expression below and simplify to obtain the minimal sum (SOP) and minimal product (POS). **08**
$f(w,x,y,z)= \sum m(0,1,2,4,5,7,9,12)$
Also, draw the logic diagram for the simplified expressions.

b) Show the working of AND gate, NOT gate and OR gate using NOR gates. **06**
Also, justify why NOR gate is termed as universal gate.

c) Suppose a 3-variable truth table has a high output for these input values: 000, 010, 100, 110. Draw the SOP circuit. **06**

OR

2 a) Using Quine McClusky method obtain the essential prime implicants for the expression given below: **10**
$f(w,x,y,z)= \sum m(2,7,9,12,14,15) + dc(0,8,13)$

b) Implement XNOR functionality using only NAND gates and using only NOR gates. Show the steps clearly. **10**

UNIT - II

3 a) Realize the given 4-variable expression using 8-to-1 multiplexer as well as 4-to-1 multiplexer. **08**
$f(w,x,y,z)= \sum(0,1,3,5,9,11,15)$

b) Design a 3-to-8 decoder to implement the following functions: **06**
$f_1(x_2,x_1,x_0)=\pi M(0,1,3,4,7)$
$f_2(x_2,x_1,x_0)= \pi M(1,2,3,4,5,6)$
Assume all the 8 output lines of the decoder are active low signals.
Note: Use NAND gates only for implementation.

c) Analyze and show how a 16 to 1 Multiplexer can be used to compare two 2-bit numbers, A_1A_0 and B_1B_0 to generate two outputs A>B and A=B. **06**

UNIT - III

4 a) Design a PAL with 4 inputs and 3 outputs to implement the following **08**

functions:
$F_1(A,B,C) = \Sigma\, m(0,3,4,5,6)$
$F_2(A,B,C) = \Sigma\, m(1,3,5,6,7)$
$F_3(A,B,C) = \Sigma\, m(0,4,5)$

b) Design a 3*4*2 PLA for the following functions: **08**
$f_1(x,y,z)=\sum m(1,2,3,7)$
$f_2(x,y,z)= \sum m(0,1,2,6)$
Use XOR gates to show the true and complemented form of output functions.

c) Draw a PROM for the following functions: **04**
$f_1(x,y,z)=\sum m(0,1,2,5,7)$
$f_2(x,y,z)= \sum m(1,2,4,6)$

UNIT - IV

5 a) Design a synchronous mod-6 counter using JK flip-flops for the following counting sequence: **10**
000, 101, 001, 111, 011, 100, and then back to 000

b) Design a JK Flip Flop using RS Flip Flop. Represent the RS Flip Flop as well as JK Flip Flop using state transition diagram. Also, design the excitation table using the constructed state transition diagram. **06**

c) A fictitious flip-flop with 2 inputs A and B functions as follows. For AB = 00 and AB = 11, the output becomes 0 and 1 respectively. For AB = 01 flip-flop retains previous output, while for AB = 10, flip-flop complements previous output. Derive the truth table, excitation table, characteristic equations and state transition diagram for this fictitious flip-flop. **04**

UNIT - V

6 a) Differentiate between Moore and Mealy models for designing synchronous sequential circuits. **05**

b) Design a synchronous sequential logic circuit using Mealy model that detects a sequence 101 from an input data stream X: (in non-overlapping form: i.e. Input:0110101011001 and corresponding Output: 0000100010000) and signals detection by making output, Z = 1. Use D Flipflops for final circuit realization. **10**

c) Differentiate between combinational and sequential circuits with an example for each. **05**

OR

7 a) Design a synchronous sequential circuit: Mealy model for the following problem statement: **10**
Design a binary sequence detector with input X and output Y. the output is made high or 1 when the following input combination "101" is given. For all other cases the output is low or 0.

b) Design a sequence detector using Moore model that searches for a series of binary inputs to satisfy the pattern 01[0*]1, where [0*] is any number of consecutive zeroes. The output (Z) should become true every time the sequence is found. **10**

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