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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 22CS3PCLOD **Max Marks: 100**
Course: Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Simplify the logic expression using K-map and implement the logic circuit using basic gates. **06**
F(a,b,c,d)=∑m(0,1,2,3,4,6,8,9,10,11,12,14)

b) Simplify the logic expression using K-map to obtain the POS: **06**
πM(0,1,2,4,8,9,15) + dc(11,14)

c) Simplify F(w, x, y, z)= ∑m(1,4,6,7,8,9,10,11,15) using Quine McCluskey Method. **08**

OR

2 a) For the given Boolean expression, F(w,x,y,z)=xy'z+x'y'z+w'xy+wx'y+wxy **08**
i. Obtain the truth table of F
ii. Draw the logic diagram using the original Boolean expression.
iii. Use Boolean Algebra to simplify the function to a minimum number of literals.
iv. Draw the logic diagram of the simplified Boolean expression using
a. NAND gates only
b. Basic gates only
v. Give comparison for the total number of gates used in both cases. (NAND gates only and Basic Gates Only)

b) Convert each of the following to the other canonical form and implement the resulting function using minimum number of universal gates. Use K-Maps. **08**
(i)F(A,B,C,D)= ∑(0,6,8,13,14)
(ii)F(W,X,Y,Z)=π(0,1,2,4,7,9,12)

c) Differentiate between Prime Implicants and essential Prime Implicants with the help of an example. **04**

UNIT - II

3 a) Assume that a room has three doors and a switch by each door to control a single light in the room. Let X, Y and Z denote the state of all the switches. **06**

Assume the light is off if all the switches are open. Closing any switch turns the light ON, but closing another switch will turn the light OFF. Light is ON if all three switches are closed. Construct a truth table and implement the logic using 2 to 1 multiplexer along with minimum possible number of gates.

b) Realize the given 4-variable expression using 8-to-1 multiplexer as well as 4-to-1 multiplexer. **06**
$f(w,x,y,z)= \sum m(0,1,3,5,9,11,15)$

c) Analyze and show how a 16 to 1 Multiplexer can be used to compare two 2-bit numbers, A_1A_0 and B_1B_0 to generate two outputs A>B and A=B. **08**

UNIT - III

4 a) List the different types of PLD's with their general structure. **6**

b) Realize the following function using PROM: **6**
$F1(x,y,z)= \sum m(0,2,4)$
$F2(x,y,z)= \sum m(1,3,4,5,7)$

c) Realize the given function using PAL: **8**
i)$X(A,B,C)=\sum m(2,3,5,7)$
ii)$Y(A,B,C)= \sum m(0,1,5)$
iii) $Z(A,B,C)= \sum m(0,2,3,5)$

UNIT - IV

5 a) Define sequential circuit. Explain the operation of SR latch with circuit, characteristic table, characteristic equation and timing diagrams. **10**

b) Draw the logic circuit for Master-Slave JK Flip Flop and explain its operation with waveforms. **10**

UNIT - V

6 a) Design a 3-bit asynchronous down counter. Also write the input output waveforms **07**

b) Design a synchronous counter using JK flip flops to count the sequence, 000---001---010---100---101---110---000 **08**

c) Differentiate between combinational and sequential circuits with an example for each. **05**

OR

7 a) Design a mod 8 synchronous up counter. Write the input and output waveforms. Also write the applications of a counter. **10**

b) Design a synchronous sequential circuit: Mealy model for the following problem statement: **10**
Design a binary sequence detector with input X and output Y. the output is made high or 1 when the following input combination "101" is given. For all other cases the output is low or 0.

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