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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E.

Branch: Computer Science and Engineering

Course Code: 22CS3PCLOD

Course: Logic Design

Semester: III

Duration: 3 hrs.

Max Marks: 100

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			UNIT - I			CO	PO	Marks
Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.	1	a	Construct truth table for each of the following Boolean functions i) $F(A, B, C) = (A'+B)(B'+C)$ ii) $F(A, B, C) = AB + BC + CA$		CO1	PO1	06	
		b	Draw the logic diagram using gates corresponding to the following Boolean expressions. Assume that the input variables are available in both complemented and uncomplemented form. i) $Y = A'B'C' + AB + AC$ ii) $A = X(YZ' + Y'Z) + W'(Y' + X'Z)$		CO1	PO1	06	
		c	Draw the truth table for the logical function M for three inputs A, B and C, where $M = F(A, B, C)$. The output is 0 (zero), if the majority of inputs are zero (0) and one (1) if the majority of inputs are one (1). Write the sum of products expression (SOP) and circuit diagram for M.		CO2	PO2	08	
			OR					
	2	a	Simplify the following Boolean functions to obtain minimal sum expressions. i) $F(a,b,c,d) = \sum m(0,2,5,7,8,10,13,15) + \sum d(1,4,11,14)$ ii) $F(a,b,cd) = \pi M(0,1,4,5,8,9,11) + \pi d(2,10)$		CO1	PO1	10	
		b	Using Quine-McCluskey method, obtain all the prime implicants for the following Boolean function: $f(a,b,c,d) = \sum m(0,1,2,5,6,7,8,9,10,14)$		CO1	PO1	10	
			UNIT - II					
	3	a	Implement the Boolean function $f(a,b,c,d) = \sum m(4,5,7,8,10,12,15)$ using a 4 to 1 line MUX and external gates if i) a and b are connected to select lines a1 and a0 respectively ii) c and d are connected to select lines a1 and a0 respectively		CO3	PO3	10	
		b	Implement the given function using 3 -to-8-line decoder using OR gates $f1(x,y,z) = \sum m(2,3,5,6)$ $f2(x,y,z) = \sum m(1,4,5,6)$		CO3	PO3	04	

	c	Design a 1- bit magnitude comparator using basic gates.	CO3	PO3	06																																																																																																
		UNIT - III																																																																																																			
4	a	Design a BCD to Excess-3 code converter and implement it using a suitable PLA.	CO3	PO3	10																																																																																																
		<table border="1"> <thead> <tr> <th colspan="4">Input (BCD Code)</th> <th colspan="4">Output (Excess-3 Code)</th> </tr> <tr> <th>B₃</th> <th>B₂</th> <th>B₁</th> <th>B₀</th> <th>E₃</th> <th>E₂</th> <th>E₁</th> <th>E₀</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> </tbody> </table>	Input (BCD Code)				Output (Excess-3 Code)				B ₃	B ₂	B ₁	B ₀	E ₃	E ₂	E ₁	E ₀	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	0	0	1	0	0	1	0	1	0	0	1	1	0	1	1	0	0	1	0	0	0	1	1	1	0	1	0	1	1	0	0	0	0	1	1	0	1	0	0	1	0	1	1	1	1	0	1	0	1	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0			
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	b	Implement the Boolean functions $F1 = A'BC'D + A'BCD' + ABC'D$ and $F2 = A'BC' + A'BC + AB'C + ABC'$ with PAL device.	CO3	PO3	10																																																																																																
		UNIT - IV																																																																																																			
5	a	With the help of circuit diagram, derive the truth table, characteristic equation and timing diagram of SR Flip Flop.	CO2	PO2	10																																																																																																
	b	List different types of registers. Explain serial in parallel out register with neat diagram.	CO2	PO2	07																																																																																																
	c	Explain working of simple bistable element with diagram.	CO2	PO2	03																																																																																																
		UNIT - V																																																																																																			
6	a	Design a Mod-6 synchronous counter using JK flip-flops.	CO3	PO3	10																																																																																																
	b	Design a 3 bit binary ripple counter that counts up using JK Flip Flop and explain the working.	CO3	PO3	10																																																																																																
		OR																																																																																																			
7	a	Design sequence detector using moore model so that any input sequence ending in 011 will produce an output Z = 1. Use JK Flip-flops for final circuit realization.	CO3	PO3	10																																																																																																
	b	With a block diagram compare mealy and moore model. Construct state synthesis table for given state transition diagram.	CO2, 3	PO2, 3	10																																																																																																

7b)


