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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 22CS3PCLOD **Max Marks: 100**
Course: Logic Design **Date: 19.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Analyze the given Truth Table. Reduce it to SOP and draw the logic diagram. **6**

X	Y	Z	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

b) Given the Boolean function, determine a minimal sum and minimal product using K-maps where w, x, y, z are variables. **6**
f (w, x, y, z) = ∑m (2,3,4,10,13,14,15) + dc (7,9,11)

c) Using Quine McClusky method obtain the essential prime implicants for the expression given below. **8**
f (A, B, C, D) = ∑m (0,2,3,6,7,8,10,12,13)

OR

2 a) Design a SOP circuit which accepts 3 inputs a, b and c and outputs a 1(HIGH) when input has exactly two 1's. **6**

b) Given the Boolean function, determine a minimal sum and minimal product using K-maps where w, x, y, z are variables. **6**
f (w, x, y, z) = πM (0,1,2,4,10,11,15) + dc (3,8,9)

c) Simplify f(w,x,y,z)=∑m(0,5,6,7,9,10,13,14,15) using Quine McCluskey method. **8**

UNIT - II

3 a) Assume an adder/subtractor which is capable of handling two 4-bit operands. For each of the following set of unsigned operands, X &Y, and control input Add/Sub, determine the output. Check your answers by converting the binary numbers into decimal. **6**

i) X=0101, Y=0011, Add/Sub=0
ii)X=0101, Y=0011, Add/Sub=1
Draw the logic diagram using parallel binary adder /subtractor using X-OR gate.

b) Using 3-to-8 decoder realize the following pairs of expressions. In each case gates should be selected as to minimize their total number of input terminals. **6**

i) $f_1(x_2,x_1,x_0)= \sum m\ (1,2,4,5)$
$f_2(x_2,x_1,x_0)= \sum m\ (0,1,3,4,5,6)$

ii) $f_1(_{x2},x_1,x_0)= \pi m\ (0,3,5)$
$f_2(x_2,_{x1},x_0)= \pi m\ (1,2,3,4,5,6)$

c) Realize each of the following Boolean expressions **8**

i) using an 8-to-1 line multiplexer where w,x,and y appear on select lines S_2, S_1 and S_0 respectively
$f(w,x,y,z)= \sum m(0,4,6,8,9,11,13,14)$

ii) using 4-to-1 line multiplexer and external gates implement
$f(w,x,y,z)= \sum m(4,5,7,8,10,12,15)$
Let w and x appear on the select lines S_1 and S_0 respectively.

UNIT - III

4 a) Explain Programmable Array Logic with a neat diagram. **6**

b) Design the PROM for the following function. **6**
$f_1(x,y,z)= \sum m(0,1,2,5,7)$
$f_2(x,y,z)= \sum m(1,2,4,6)$

c) Design a PLA 4x5x2 i.e 4 inputs, 5 AND gates and 2 OR gates for the following functions. **8**
$f_1(w,x,y,z)= \sum m(2,4,5,10,12,13,14)$
$f_2(w,x,y,z)= \sum m(2,9,10,11,13,14,15)$

UNIT - IV

5 a) List the different types of Registers. Explain Serial In Parallel Out with neat diagram. **6**

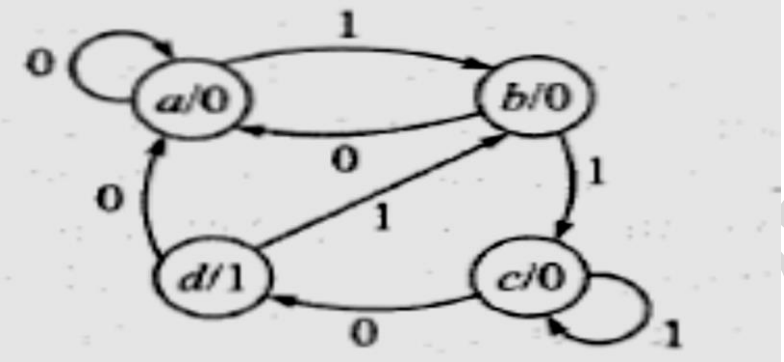
b) Explain the working of Master-Slave JK flip flop with timing diagram. **6**

c) Derive the characteristic equation for SR flip flop, JK flip flop and D flip flop. **8**

UNIT - V

6 a) Design a MOD-6 synchronous up counter using JK flip flop **10**

b) Given the state transition diagram using Moore Model design the sequence detector that receives the binary data with the pattern '011'. **10**
Note: Consider data coming from Left to Right



OR

7 a) Design a synchronous up counter using JK flip flop for the given sequence 2,3,7,5,6,4 **10**

b) Design a sequence detector that receives binary data stream at its input X and signals when a combination '011' arrives at the input by making its output , Y high which otherwise remains low. Consider data coming from Left to Right i.e first bit to be identified is 1, second 1 and third 0 from the input sequence. Design the above sequence detector using Mealy Model. **10**

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