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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

April 2024 Semester End Main Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 23CS3PCLOD **Max Marks: 100**
Course: Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Suppose a 3-variable truth table has high output for these input values:000, 010, 100, 110. Draw the SOP circuit	CO1	PO1	**6**
	b)	Implement the K-Map for the given Boolean expression. Obtain the minimal sum (SOP) and minimal product(POS). Using Quine McClusky method obtain the essential prime implicants for the expression given below. f (w,x,y,z) = ∑m (0,1,2,4,5,7,9,12)	CO2	PO2	**6**
	c)	Using Quine McClusky method obtain the essential prime implicants for the expression given below. f (w,x,y,z) = ∑m (2,7,9,12,14,15) + dc(0,8,13)	CO2	PO2	**8**
		OR			
2	a)	Design a SOP circuit which accepts 3 inputs a, b and c and outputs a 1(HIGH) when input has exactly two 1's.	CO1	PO1	**6**
	b)	Given the Boolean function, determine a minimal sum and minimal product using K-maps where w, x, y, z are variables. f (w, x, y, z) = ∑m (2,3,4,10,13,14,15) + dc (7,9,11)	CO2	PO2	**6**
	c)	Using Quine McClusky method obtain the essential prime implicants for the expression given below. f (A, B, C, D) = ∑m (0,2,3,6,7,8,10,12,13)	CO2	PO2	**8**
		UNIT - II			
3	a)	Realize each of the following Boolean expressions using an 8-to-1 line multiplexer choosing a, b and c as select lines f(a,b,c,d)= ∑m(0,1,5,6,7,9,10,15)	CO2	PO2	**6**
	b)	i. Using 3-to-8 decoder realize the following pairs of expressions. f1(a,b,c)= ∑m (0,2,3,5,6,7) f2(a,b,c)= ∑m (1,3,4,6,7)	CO2	PO2	**6**

			ii. Using 3-to-8 decoder realize the following pairs of expressions with active low outputs and AND gates. f1(a,b,c)= πM (0,1,3,5,6) f2(a,b,c)= πM (2,3,4,5,7)			
		c)	Design a 2-bit comparator that compares the magnitude of two binary numbers (i.e greater than, less than and equal to the other) with truth table and neat logic diagram.	*CO3*	*PO3*	**8**
			UNIT - III			
	4	a)	Design the PROM for the following function. f1(x,y,z)= ∑m(0,1,2,5,7) f2(x,y,z)= ∑m(1,2,4,6)	*CO3*	*PO3*	**4**
		b)	Design a 3x4x2 PLA i.e 3 inputs, 4 AND gates and 2 OR gates for the following functions. f1(w,x,y,z)= ∑m(1,2,3,7) f2(w,x,y,z)= ∑m(0,1,2,6) Use XOR gate to show the true and complemented form of the function.	*CO3*	*PO3*	**8**
		c)	Design the PAL with 4-inputs and 3-outputs to implement the following function. f1(A,B,C)= ∑m(0,3,4,5,6) f2(A,B,C)= ∑m(1,3,5,6,7) f3(A,B,C)= ∑m(0,4,5)	*CO3*	*PO3*	**8**
			UNIT - IV			
	5	a)	Illustrate the working of basic bi-stable element with neat diagram.	*CO1*	*PO1*	**6**
		b)	Explain the working of Master-Slave JK flip flop with neat timing diagram.	*CO1*	*PO1*	**6**
		c)	Derive the characteristic equation for SR flip-flop, JK flip flop and D flip flop.	*CO2*	*PO2*	**8**
			UNIT - V			
	6	a)	Explain Combinational circuit and Sequential circuit with example.	*CO1*	*PO1*	**6**
		b)	Differentiate between Mealy model and Moore model	*CO2*	*PO2*	**6**
		c)	Design a MOD-6 synchronous up-counter using JK flip flop.	*CO3*	*PO3*	**8**
			OR			
	7	a)	Design a synchronous up-counter using JK flip flop for the given counting sequence. 000, 101, 001, 111, 011, 100	*CO3*	*PO3*	**10**
		b)	Design a sequence detector that receives binary data stream at its input X and signals when a combination '011' arrives at the input by making its output , Y high which otherwise remains low. : Consider data coming from Left to Right i.e first bit to be identified is 1, second 1 and third 0 from the input sequence. Design the above sequence detector using Mealy Model.	*CO3*	*PO3*	**10**

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