U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June / July 2024 Semester End Make-Up Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science & Engineering **Duration: 3 hrs.**
Course Code: 23CS3PCLOD **Max Marks: 100**
Course: Logic Design

Instructions: 1.Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	*CO*	*PO*	Marks
1	a)	Analyze the following the following scenario: There are 3 inputs x,y,z and 3 outputs a,b,c. When the binary input is 0,1,2,3 the binary output is one greater than the respective input. When binary input is 4,5,6,7 the binary output is one less than the respective binary input. Outline a truth table for this problem and design a simple circuit diagram using separate k maps for each output.	*CO2*	*PO2*	**8**
	b)	Sketch the Karnaugh map for the given example and find the simplified boolean expression by solving K-maps i) F (A, B, C, D) = ∑m(0, 2, 5, 7, 8, 10, 13, 15) ii) F (P, Q, R) = π(0,3,6,7)	*CO3*	*PO3*	**8**
	c)	Explain POS and SOP in K-maps with suitable examples.	*CO2*	*PO2*	**4**
		OR			
2	a)	Describe the steps to find both the minimal sum-of-products (SOP) and product-of-sums (POS) expressions using K-maps with don't-care conditions with example.	*CO3*	*PO3*	**8**
	b)	Using Quine McClusky method obtain the prime implicants for the following. Also indicate the essential prime implicants f (w,x,y,z) = ∑m (2,7,9,12,14,15) + dc(0,8,13)	*CO2*	*PO2*	**8**
	c)	Analyze the following truth table. Express it in the form of SOP. Give the relevant logic diagram using basic gates.	*CO1*	*PO1*	**4**

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

			UNIT - II			
	3	a)	Describe combinational circuits? Give the design for 2-bit comparators with relevant truth table and K maps.	*CO2*	*PO2*	**8**
		b)	Realize the given 4-variable expression using f(a,b,c,d)= ∑m(4,5,7,9,11,12,13,15) i) An 8-to-1 line multiplexer choosing a,b,c as select lines ii) An 4-to-1 line multiplexer where a and b are select lines.	*CO3*	*PO3*	**8**
		c)	Briefly explain encoder and decoder.	*CO1*	*PO1*	**4**
			UNIT - III			
	4	a)	Describe Programmable logic devices and provide the general structure. Realize the following Boolean expressions using a PROM. (i) $f1(a,b,c) = \sum m(0,1,2,5,7)$ (ii) $f2(a,b,c) = \sum m(1,2,4,6)$	*CO3*	*PO3*	**8**
		b)	Design the following using 3*4*2 PLA. *f1(a,b,c) =∑m(0,1,3,5) f2(a,b,c) =∑m(3,5,7)*	*CO3*	*PO3*	**8**
		c)	Outline the Differences between the three programmable logic devices.	*CO3*	*PO3*	**4**
			UNIT - IV			
	5	a)	Explain undefined or forbidden state in SR flip-flop	*CO1*	*PO1*	**5**
		b)	Compare the working of SR flip flops and JK flip flops using timing diagram.	*CO3*	*PO3*	**10**
		c)	Describe the Behavior and characteristics of D and JK flip flops using appropriate equations.	*CO2*	*PO2*	**5**
			UNIT - V			
	6	a)	Demonstrate the working of binary ripple counter with timing diagram? Explain its disadvantages	*CO3*	*PO3*	**5**
		b)	Describe the steps to design a 3-bit Synchronous Counter using JK Flip-Flops	*CO2*	*PO2*	**10**
		c)	Explain Mealy and Moore model with any simple example	*CO2*	*PO2*	**5**
			OR			
	7	a)	Design a sequence detector using Moore model that searches for a series of binary input to satisfy the pattern 01[0*]1, where [0*] is any number of 0's. The output (Z) should become true every time the sequence is found.	*CO2*	*PO2*	**10**
		b)	Design a self-correcting modulo-6 synchronous counter in which all unused state leads to state CBA=000 using JK Flip-flop.	*CO3*	*PO3*	**10**

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