U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: III**

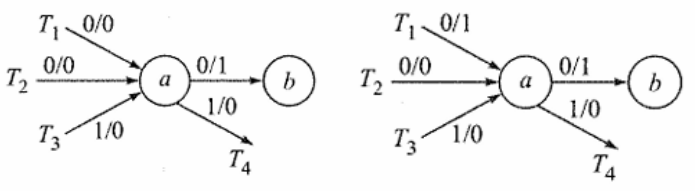
Branch: Computer Science and Engineering **Duration: 3 hrs.**

Course Code: 23CS3PCLOD / 22CS3PCLOD **Max Marks: 100**

Course: Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

			UNIT - I	*CO*	*PO*	Marks
1	a)		Simplify using K map Y(a,b,c,d)=∑m(7,9,10,11,12,13,14,15)	*CO2*	*PO2*	**10**
	b)		Simplify the equation Y=(A+B) ((A'(B'+C'))'+A'(B+C)	*CO2*	*PO2*	**5**
	c)		With neat diagram and truth table explain basic gates.	*CO1*	*PO1*	**5**
			OR			
2	a)		Minimize using Quine McClusky method. Y(A,B,C,D)=∑(0,1,2,3, 10,11,12,13,14, 15)	*CO1*	*PO1*	**10**
	b)		Prove that A(A'+C)(A'B+C)(A'BC+C')=0	*CO1*	*PO1*	**5**
	c)		Write Y(A,B,C)=A'B'C' +A'BC+AB'C+ABC as Sum of product and Product of Sum.	*CO2*	*PO2*	**5**
			UNIT - II			
3	a)		Realize function Y(A,B,C,D)=∑(0,2,3,4,5,8,9,10,11,12,13,15) using 8:1 multiplexer.	*CO2*	*PO2*	**6**
	b)		Realize 16:1 multiplexer using 4:1 multiplexer with suitable examples.	*CO2*	*PO2*	**6**
	c)		Design 4:1 multiplexer using basic gates.	*CO2*	*PO2*	**8**
			OR			
4	a)		Design 2:4 decoder.	*CO2*	*PO2*	**6**
	b)		Realize f1=∑m(0,4,6) and f2=∑m(0,5) using 3:8 decoder.	*CO2*	*PO2*	**6**
	c)		Design BCD to decimal decoder.	*CO2*	*PO2*	**8**

			UNIT - III			
	5	a)	Realize F1(a,b,c)=∑m(0,1,3,5,7) and F2(a,b,c)=∑m(1,2,5,6) using PROMs.	*CO2*	*PO2*	**6**
		b)	Compare different programmable devices.	*CO1*	*PO1*	**6**
		c)	Explain structure of PAL?	*CO2*	*PO2*	**8**
			OR			
	6	a)	Realize A=XY+XZ' and B= XY'+ YZ + XZ' using PLA.	*CO2*	*PO2*	**6**
		b)	Realize A=XY+XZ' and B= XY' +YZ' using PAL.	*CO2*	*PO2*	**6**
		c)	With a neat diagram explain structure of PROM.	*CO1*	*PO1*	**8**
			UNIT - IV			
	7	a)	Design SR latch using NOR gates.	*CO3*	*PO3*	**6**
		b)	Derive characteristic equation for JK FF.	*CO3*	*PO3*	**6**
		c)	Design positive edge triggered JK flip flop. Also write truth table and timing diagram.	*CO3*	*PO3*	**8**
			OR			
	8	a)	Derive characteristic equation for SR Flip flop.	*CO3*	*PO3*	**6**
		b)	Design SR flip flop with enable input.	*CO3*	*PO3*	**6**
		c)	How Master slave JK flip flop overcomes the toggling of JK flip flop.	*CO3*	*PO3*	**8**
			UNIT - V			
	9	a)	Design 3-bit ripple counter.	*CO3*	*PO3*	**6**
		b)	Compare mealy and Moore machines	*CO3*	*PO3*	**6**
		c)	Design mod6 synchronous counter using JK flip flops.	*CO3*	*PO3*	**8**
			OR			
	10	a)	Design 3bit up/down counter using JK flip flops.	*CO3*	*PO3*	**6**
		b)	Convert the given mealy machine to Moore machine. 	*CO3*	*PO3*	**6**
		c)	Design Mealy machine to check for 011 in the bit stream.	*CO3*	*PO3*	**8**

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