U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Computer Science and Engineering **Duration: 3 hrs.**
Course Code: 23CS3PCLOD **Max Marks: 100**
Course: Logic Design

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

		UNIT - I	CO	PO	Marks
1	a)	Construct truth table for each of the following Boolean functions i) F(x,y,z)= x'y+xz ii) F(a,b,c)= (a'+b)(b+c')	CO2	PO2	5
	b)	A switching circuit has four inputs(C1, C2, X1, X2) where C1 and C2 are control inputs. X1 and X2 are data inputs. There is one output Z. The circuit performs one of the logic operations AND, OR, EQU(equivalence) ,XOR (exclusive OR) on the two data inputs. The function performed depend on the control inputs: C1 | C2 | Function Performed by Circuit 0 | 0 | OR 0 | 1 | XOR 1 | 0 | AND 1 | 1 | EQU (i) Derive a truth table for Z (ii) Use a K-map to find a minimum AND-OR gate circuit to realize Z.	CO3	PO3	10
	c)	Show the working of AND gate, NOT gate and OR gate with respective truth table. Also, justify why NAND gate is termed as universal gate.	CO2	PO2	5
		OR			
2	a)	Simplify the following Boolean functions to obtain minimal sum using karnaugh maps. (i) $f(w, x, y, z) = \sum m(6,7,9,10,13) + dc(1,4,5,11,15)$ (ii) $f(w, x, y, z) = \pi\, m(1,2,3,9,10) + dc(0,4,14,15)$	CO1	PO1	10
	b)	Using Quine-McCluskey method, obtain all the prime implicants for the following Boolean function: f(a,b,c,d) = $\sum m(2,3,7,9,11,13) + \sum dc(1,10,15)$	CO1	PO1	10

			UNIT - II			
	3	a)	Realize the given 4-variable expression using f(a,b,c,d)= ∑m(4,5,7,9,11,12,13,15) i) An 8-to-1 line multiplexer where a, b and c are select lines. ii) An 4-to-1 line multiplexer where a and b are select lines.	*CO3*	*PO3*	**10**
		b)	Design the realization of 8-to-3 line encoder. Extend the logic to realize 8-to-3 line priority encoder.	*CO3*	*PO3*	**10**
			UNIT - III			
	4	a)	Describe Programmable logic devices and provide the general structure. Realize the following Boolean expressions using a PROM. (i) $f1\ (x2, x1, x0) = \sum m(0,1,2,5,7)$ (ii) $f2\ (x2, x1, x0) = \sum m(1,2,4,6)$	*CO3*	*PO3*	**10**
		b)	Design the following functions using PLA with 3 inputs, 3 product terms, 2 output and show the PLA table. i) f1(a,b,c)=∑m(4,5,7) ii) f2(a,b,c)= ∑m(3,5,7)	*CO3*	*PO3*	**10**
			UNIT - IV			
	5	a)	Summarize the working of a Master Slave JK Flip-flop with the help of a logic diagram, timing diagram and truth table.	*CO2*	*PO2*	**10**
		b)	Derive the characteristics equation for SR and D Flip-flops.	*CO2*	*PO2*	**10**
			UNIT - V			
	6	a)	Design a self-correcting modulo-6 synchronous counter in which all unused state leads to state CBA=000 using JK Flip-flop.	*CO3*	*PO3*	**10**
		b)	Design a 3 bit binary ripple counter that counts up using JK Flip Flop and explain the working.	*CO3*	*PO3*	**5**
		c)	Differentiate between combinational circuits and sequential circuits with example for each.	*CO2*	*PO2*	**5**
			OR			
	7	a)	Design a sequence detector using Moore model, that receives binary stream at its input, X and signals when a combination '011' arrives at the input by making its output, Y high which otherwise remains low. Consider the data is coming from left i.e. the first bit to be identified is 1, second 1 and third 0 from the input sequence.	*CO3*	*PO3*	**10**
		b)	Compare Moore and Mealy models for designing synchronous sequential circuits.	*CO2*	*PO2*	**5**
		c)	Write the mealy model state diagram to detect the sequence 101.	*CO2*	*PO2*	**5**

****