UNIT - I

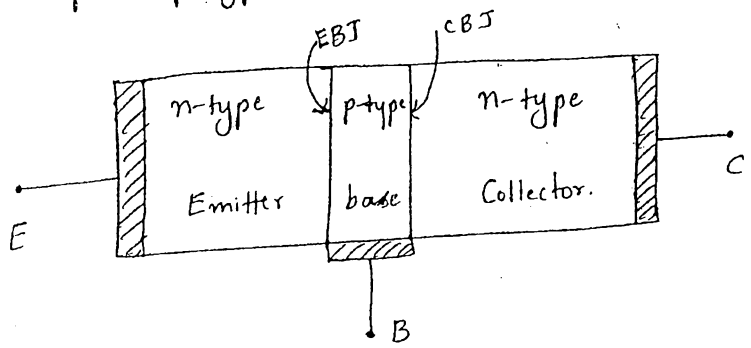
TRANSISTORS.

* BJT (Bipolar Junction transistor) Consists of two coupled p-n junctions., connected back to back with a common middle layer.
* Transistor is a contraction of word 'transfer resistor', i.e, it transfere the signal from region of low resistance to the region of high resistance.
* BJT is widely used in discrete circuits as well as IC design (both analog and digital) hence these devices widely used in variety of applications ranging from signal amplification to the design of digital logic and memory circuits.
* BJT is a three layered device with two junctions. and can provide circuit properties amplification and switching.

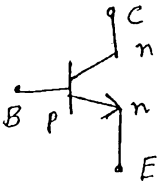
Physical Structure and Modes of operation

* An npn BJT has a thin p-type region placed between two n-type regions. It has three semiconductor regions emitter region ~~box~~ (n type), base region (p-type) & collector (n type)

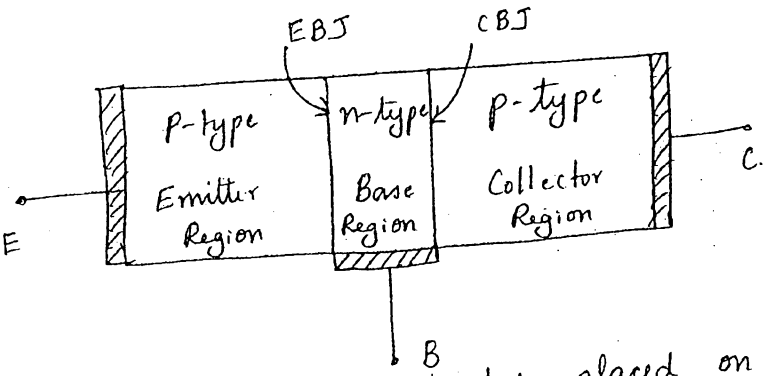
* Another type of transistor is pnp ... consists of p-type emitter, n-type base and p-type collector

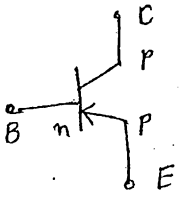


Circuit Symol



① n-p-n Transistor





* In circuit symol arrow head is placed on the emitter, and its direction represents the direction of conventional current (flow of holes)
* The doping level of three regions are different, emitter region is heavily doped, base region is lightly dope and collector region is moderately doped.
* In a transistor, the collector region is made physically larger than other two as it is required to desipate more heat.
The base is very thin.
* BJT consists of two p-n junctions known as Emitter Base Junction (EBJ) and Collector base Junction (CBJ)

* Depending on the bias condition of these junctions different modes of operation of BJT are obtained.

There are 4 possible ways of biasing these junctions.

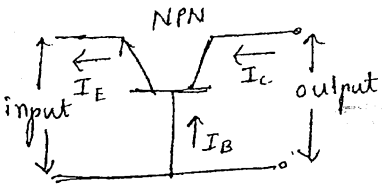
Modes of operation	EBJ	CBJ	Application
① Active	Forward biasing	Reverse biasing	Amplifiers
② Saturation	Forward biasing	Forward biasing	Switching
③ Cut-off	Reverse biasing	Reverse biasing	Switching
④ Inverse mode.	Reverse biasing	Forward biasing	Electronic circuits o TTL

~~Principle of operation of npn transistor~~

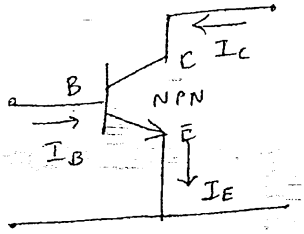
Transistor Configurations

* BJT consists of three terminals, usually to operate in a circuit we make one terminal common to both i/p input and output.

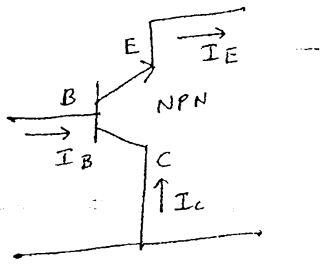
According to common terminal three are 3 configurations



Common base (CB)

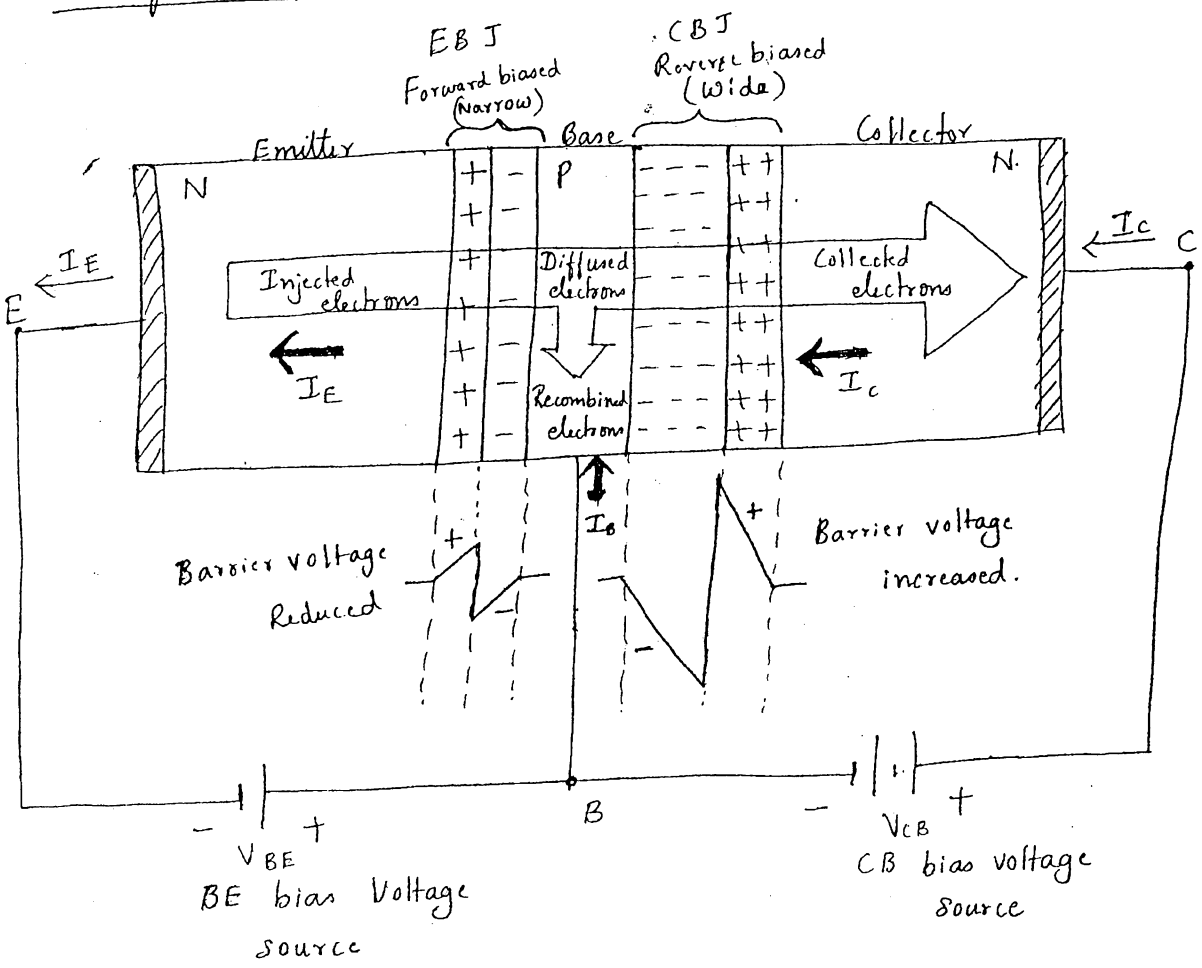


Common Emitter (CE)



Common Collector (CC)

Principle of operation of npn transistor.



* Here, CB mode is considered and transistor is operated in active mode.
* Forward biasing EBJ reduces the emitter base potential barrier, CBJ increases the collector base barrier.
* Forward bias causes electrons to flow from n-type emitter to the p-type base. Electrons are emitted into the base region, hence the name emitter
* Holes also flow from p-type base to n-type emitter, but base is lightly doped, hence ~~all~~ almost all current flow across the BE Junction. consists of electrons entering from emitter to base. In npn transistor

electrons are majority charge carriers.

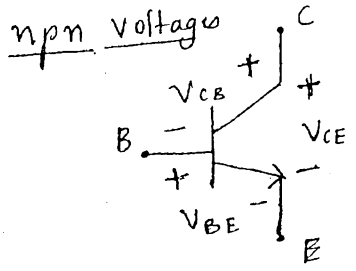
* Reverse biased CBJ makes depletion region to penetrate deeper into the base.
* Electrons crossing from emitter to base arrive much close to the large negative-positive electric field (barrier voltage) at CB depletion region.
* Electrons are drawn across the CBJ by bias voltage.
* Some electrons entering base from emitter recombine with holes and constitutes I_B (Base current)
* As base is very small in geometry & very lightly doped, 98% of charge carriers from the emitter are drawn across the CB junction to flow via the collector terminal and the voltage source back to the emitter
* In another way Reverse bias junction allows the minority charge carriers. The electrons arriving at CBJ (from emitter) appear as minority charge carriers and reverse bias assist them to flow across the junction.
* BEJ has the characteristics of forward biased diode The current will not flow until forward bias is 0.7V for Si & 0.3 V for Ge.

  Reducing the level of BE bias voltage source reduces the amount of current that flows from emitter through the base to the collector.
* ∴ Variation of small forward bias voltage V_{BE} reduces the emitter and collector currents

Note :- A pnp transistor behaves exactly the same as an npn device., ~~ex~~ with exception that majority charge carriers are holes. The direction of transistor currents are reversed ~~Hann~~ (~~flow~~ direction of flow of holes)

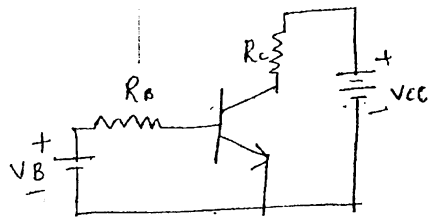
Transistor Voltages and Currents

npn Voltages



→ Along with conventional current direction the arrow head indicates bias polarities

In npn transistor arrow head points from (positive) base to the (negative) emitter.



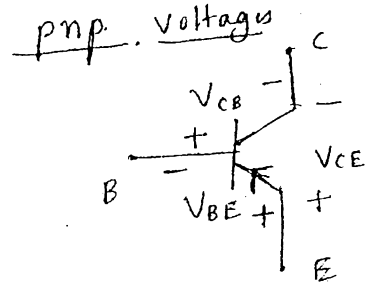
npn terminal polarities and voltage source connections

→ The collector is biased to the higher positive voltage than the base.

→ V_{CC} is always much greater than V_i

→ The sources are always connected to transistor via current limiting resistors.

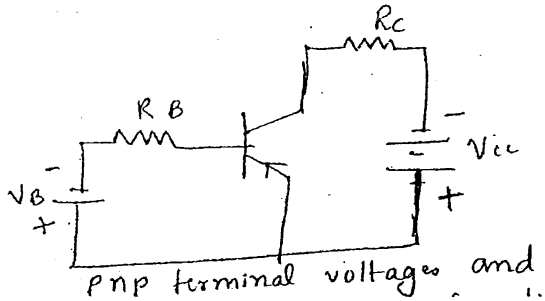
pnp Voltages



→ In pnp base is biased with respect to the emitter

→ The collector is made more negative than the base.

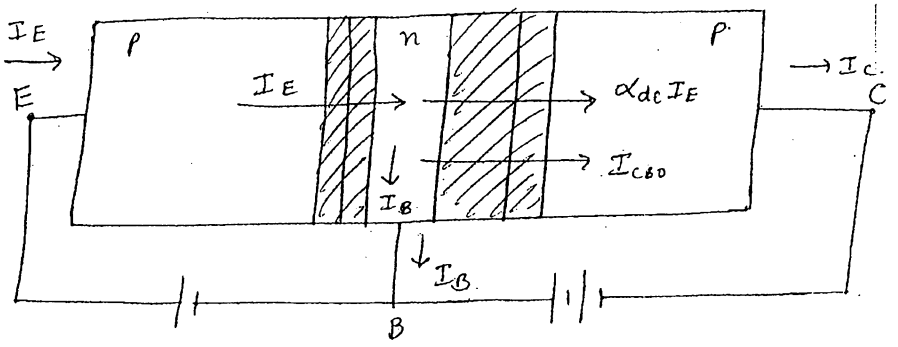
With V_{CC} more negative than V_B the collector (p-type) is more negative than base (n-type)



pnp terminal voltages and

Transistor currents

* The current flowing from emitter terminal is referred to as the emitter current, I_E.
* For a pnp transistor I_E can be thought of flow of holes from the emitter to the base. I_E flows into transistor. The base current I_B and collector current I_C are also the conventional currents flowing out of transistor.



From KCL $I_E = I_B + I_C$

* Almost all I_E crosses to the collector, only small portion flows out of the base terminal.
96% to 99.5% of I_E flows across the collector base junction, to become collector current.

$$I_C = \alpha_{dc} I_E$$

where α_{dc} is the ratio of I_C to I_E known as emitter to collector gain. α_{dc} is typically 0.96 to 0.995.

* In many circuit situations I_C is assumed equal to I_E.
* Because CB junction is reverse biased, a very small reverse saturation current flows across the junction.

* I_{CBO} is the reverse saturation current from collector to base. Normally it will be so small.

$$I_C = \alpha_{dc} \cdot (I_E) \longrightarrow (1)$$

but $$I_E = I_B + I_C \longrightarrow (2)$$

$$I_C = \alpha_{dc}(I_B + I_C) \longrightarrow (3)$$

$$I_C - \alpha_{dc} I_C = \alpha_{dc} I_B$$

$$I_C = \left[\frac{\alpha_{dc}}{1-\alpha_{dc}}\right] I_B \longrightarrow (4)$$

$$I_C = \beta_{dc} I_B \quad \text{where} \quad \beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} \longrightarrow (5) \qquad \alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

* β_{dc} is ~~collector to base~~ base to collector current gain. or the ratio of collector current to base current.

$\beta_{dc} = I_C / I_B$ and it ranges from 25 to 300.

Instead of β_{dc} another symbol used on transistor data sheet is h_{FE} (h-parameter) or ~~β_{dc}~~

* These equations (1 to 5) apply equally to npn transistor except I_B and I_C are assumed to flow ~~out of the~~ into transistor & I_E is taken as flowing out. In npn Electrons are majority charge carriers and they move in a direction opposite to the conventional current direction.

Problems on Transistor currents

(1) Determine α_{dc} and I_B for a transistor that has $I_C = 2.5\,mA$ and $I_E = 2.55\,mA$. Also calculate β_{dc} for the transistor

$$\alpha_{dc} = \frac{I_C}{I_E} = \frac{2.5\times10^{-3}}{2.55\times10^{-3}} = \underline{0.9803}$$

$$I_C = \frac{\alpha_{dc}}{1-\alpha_{dc}} I_B$$

$$I_B = \frac{(1-\alpha_{dc})}{\alpha_{dc}} I_C = \left[\frac{1-0.9803}{0.9803}\right] 2.5\times10^{-3}$$

$$\underline{I_B = 50.239\,\mu A}$$

(2) Transistor has measured current of $I_C = 3\,mA$ and $I_E = 3.03\,mA$. Calculate the new current levels when the transistor is replaced with a device that has $\beta_{dc} = 75$ Assume that I_B remains constant.

Lets calculate $I_B \Rightarrow$ $I_E = I_B + I_C$

$$I_B = I_E - I_C = 3.03\times10^{-3} - 3\times10^{-3} = \underline{30\,\mu A}$$

Assume I_B is fixed and for $\beta_{dc} = 75$

$$I_C = \beta I_B = 75 \times 30\,\mu A = \underline{2.25\,mA}$$

$$I_E = I_C + I_B = 30\,\mu A + 2.25\,mA = \underline{2.28\,mA}$$

(3) The following current measurements were made on a transistor : $I_C = 12.42\,mA$, $I_B = 200\,\mu A$. Determine I_E, α_{dc} and β_{dc}. determine a new I_C level when I_B is 150 μA.

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{12.42 \times 10^{-3}}{200 \times 10^{-6}} = \underline{\underline{62.1}}$$

$$I_E = I_C + I_B = (12.42 \times 10^{-3}) + (200 \times 10^{-6}) = \underline{\underline{12.62\,mA}}$$

$$\& \quad \alpha_{dc} = \frac{I_C}{I_E} = \frac{12.42 \times 10^{-3}}{12.62 \times 10^{-3}} = \underline{\underline{0.9841}}$$

when $I_B = 150\,\mu A$

$$I_C = \beta_{dc} I_B = 62.1 \times 150 \times 10^{-6} = \underline{\underline{9.315\,mA}}$$

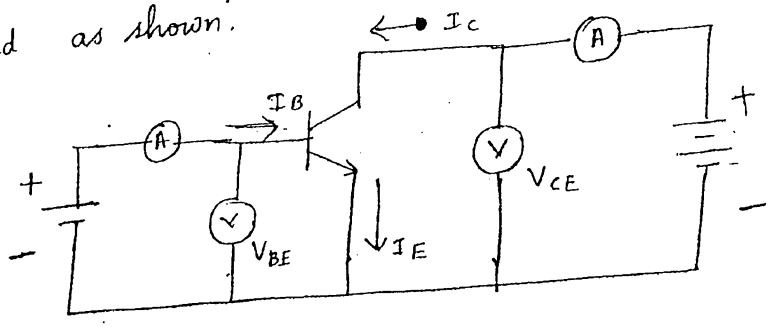
Active Region operation of a transistor.

Input characteristics: It is the curve of input current V_s input voltage when output voltage is held constant

Output characteristics: It is the curve of output current V_s output voltage when input current held constant.

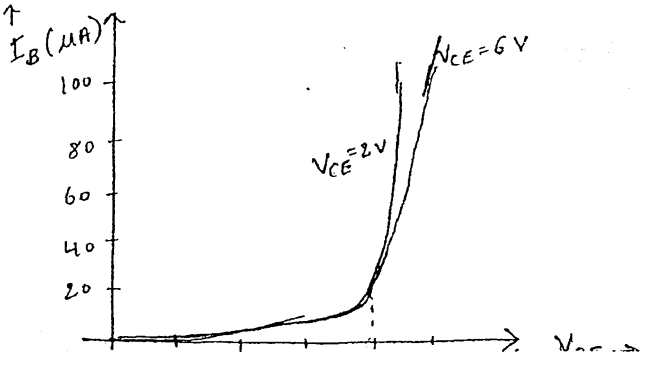
Common Emitter (CE) characteristics.

* The input voltage is applied between B and E terminal and output is taken from C and E terminals. The emitter is common to both input & output. Voltage and currents are measured as shown.



Input characteristics.

* V_{CE} is held constant, V_{BE} is set at convenient levels and corresponding I_B levels are recorded.
* I_B is then plotted Vs V_{BE}



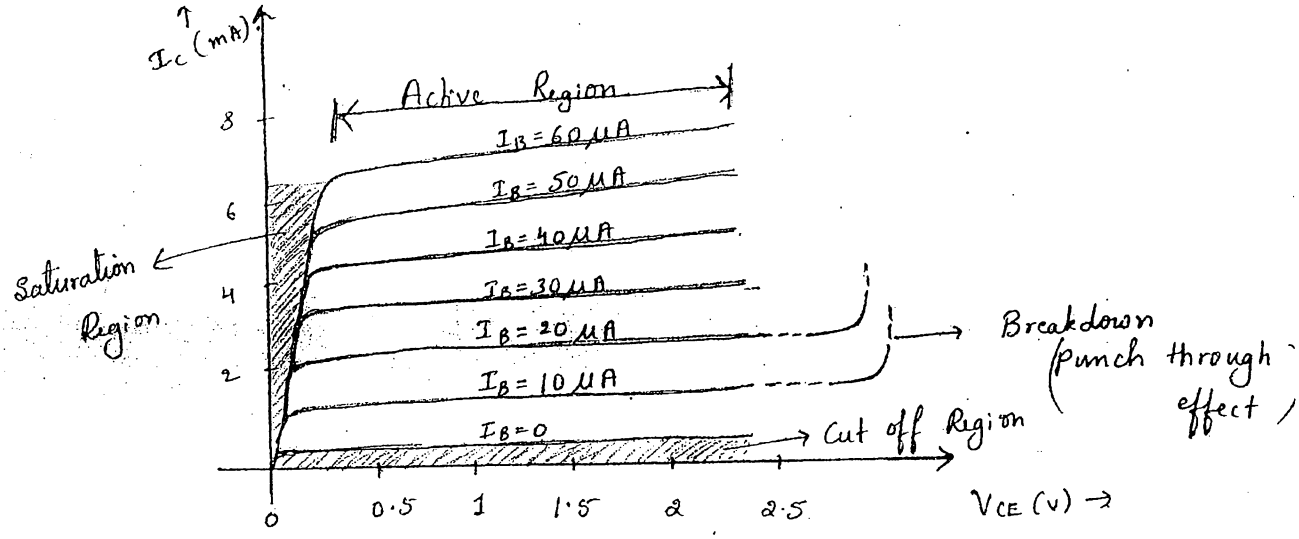
* CE input characteristics are like forward biased PN junction. I_B is a small portion of input current that flows across EBJ
* As V_{CE} increases for fixed V_{BE} I_B reduces. This is because large

CBJ, the penetration of depletion region into base increases. This reduces distance between the CB and EB depletion region Hence more charge carriers from the emitter flow across the CB junction, few flow out via the base terminal.

Output characteristics.

* I_B is maintained constant, ~~at~~ V_{CE} is adjusted in steps and I_C level is recorded at each V_{CE} step. The same procedure is repeated for several convenient levels of I_B.

I_C is plotted Vs V_{CE} to give family of characteristics.



* When V_{CE} increased, that causes V_{CB} to increase hence the distance between depletion regions shortened.. This drains more charge carriers from the emitter to collector. This increases I_C to some extent.

* The output characteristics of common emitter configuration consists of three regions. Active, Saturation & cutoff..

Saturation Region : If V_{CE} reduced to a small value such as 0.2V, the CBJ becomes forward biased. Since EBJ is already forward biased, both forward biased junctions make transistor to operate in saturation region.

The saturation value of V_{CE}, designated $V_{CE(sat)}$ usually ranges between 0.1 V to 0.3 V.

Cut off Region : The region below $I_B = 0$ is cut off region. of operation of a transistor. In this region both the junctions are reverse biased.

Active Region : The region where the curves are approximately horizontal is called "Active" region of CE configuration.

In the active region, the collector junction (CBJ) is reverse biased.

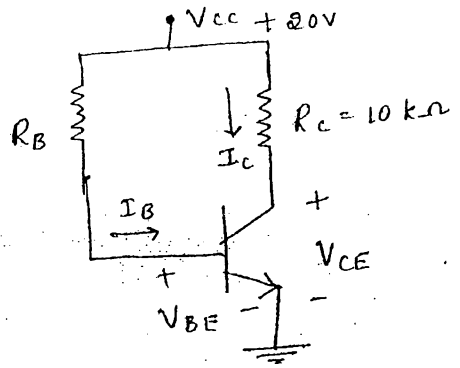
As V_{CE} is increased, reverse bias increases. This causes the depletion region to spread more in base than collector. This decreases the base region geometry and hence the recombination of carriers in base region. This causes I_C to increase sharply with increasing V_{CE}

For every transistor there is a limit on maximum value of reverse bias voltage. If this limit exceeds then breakdown occurs in transistor. This effect is shown in dashed lines, the device may get destroyed. This effect is known as punch-through effect.

Operating point and Load Line analysis of BJT

DC Load Line.

* It is the straight line drawn on the transistor output characteristics.
* For CE mode (Common Emitter), the load line is a graph of Collector current (I_C) Versus Collector-emitter voltage (V_{CE}) for given value of Collector resistance (R_C) and a given supply voltage (V_{CC})
* The load line shows all corresponding levels of I_C and V_{CE} that can exist in a particular circuit.
* Consider the common emitter circuit (Active mode)

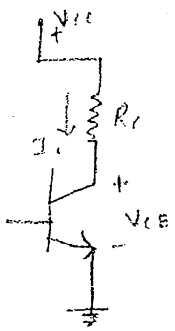


— Applying KVL to collector loop.

$$V_{CC} - I_C R_C - V_{CE} = 0 \longrightarrow (1)$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \left[\frac{-1}{R_C}\right] V_{CE} + \frac{V_{CC}}{R_C} \approx y = mx + c$$



* $I_c = (-1/R_c) V_{CE} + \frac{V_{cc}}{R_c}$ ⟶ (2)

This equation (eqn-2) resembles equation of a straight line with slope $= -1/R_c$.

* If transistor is not conducting then $I_c = 0$. From equation (2)

$$I_c = (-1/R_c) V_{CE} + \frac{V_{cc}}{R_c}$$

$I_c = 0 \Rightarrow \frac{V_{CE}}{R_c} = \frac{V_{cc}}{R_c}$

$$\boxed{V_{CE} = V_{cc}} \qquad V_{CE} = 20\,V$$

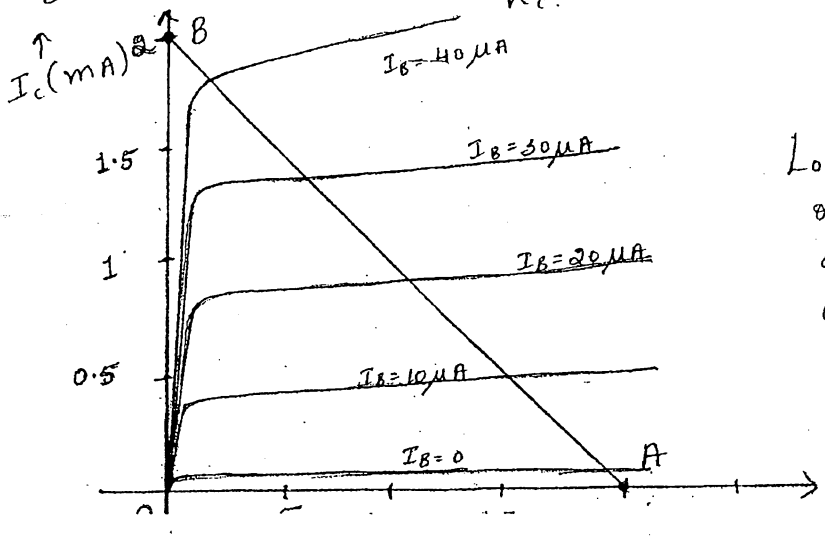
At $V_{CE} = 0V$ the equation becomes

$$I_c = (-1/R_c) V_{CE} + \frac{V_{cc}}{R_c}$$

$V_{CE} = 0 \Rightarrow \boxed{I_c = \frac{V_{cc}}{R_c}}$ $\qquad I_c = \frac{20\,V}{10\,k\Omega} = 2\,mA$

Point A ⟶ $V_{CE} = V_{cc}$ & $I_c = 0$

Point B ⟶ $V_{CE} = 0$ & $I_c = \frac{V_{cc}}{R_c}$.



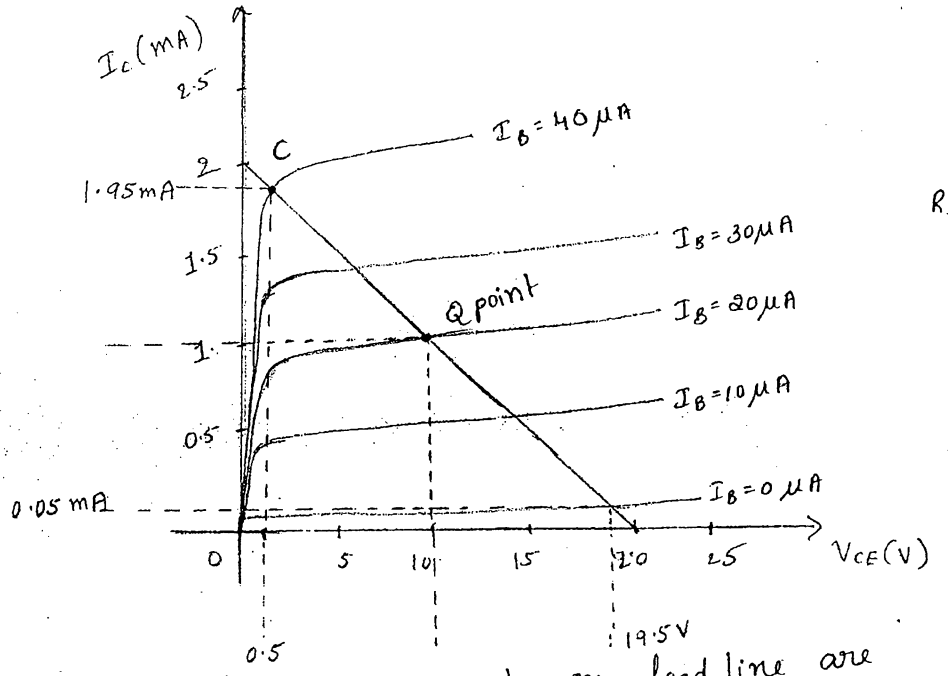
Load Line drawn on transistor CE output characteristics.

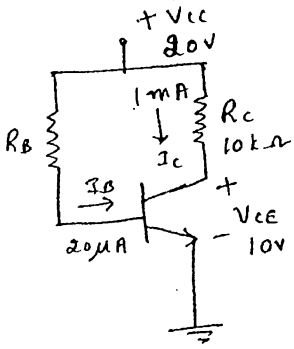
The straight line drawn through A and B is the dc load line for $R_C = 10\,k\Omega$ and $V_{CC} = 20V$. If either of these two quantities is changed, a new load line must be drawn.

* Knowing any one of I_B, I_C or V_{CE} it is easy to determine the other two from a dc load line.

DC bias point (Q-point)

* Q-point or operating point defines the dc conditions in the circuit.





$V_{CC} = I_C R_C + V_{CE}$

Bias conditions for Q-point on load line are

$I_B = 20\mu A$, $I_C = 1mA$ and $V_{CE} = 10V$

* When a signal is applied to the transistor base, I_B varies according to instantaneous amplitude of the signal. This causes I_C to vary and consequently produces a variation in V_{CE}. Hence Q point ~~shifts~~. may shift when external signal is appli

* When I_B is increased from 20 μA to 40 μA. From point Q on the load line $I_C \approx 1.95$ mA

$V_{CE} \approx 0.5$ V.

V_{CE} change from Q point is $\Delta V_{CE} = 10V - 0.5V = \underline{9.5V}$

Increasing I_B by 20 μA (from 20 μA to 40 μA) caused V_{CE} to decrease by 9.5 V (from 10V to 0.5 V)

* When I_B reduced from 20 μA to zero. From point D

$I_C \approx 0.05$ mA

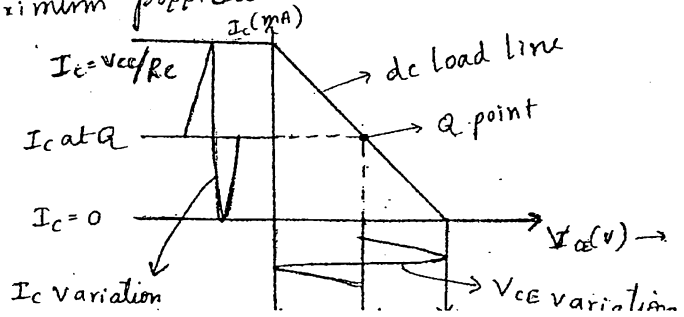
$V_{CE} \approx 19.5$ V.

V_{CE} change is $\Delta V_{CE} = 19.5 - 10 V = 9.5$ V.

Decreasing I_B by 20 μA caused V_{CE} to increase by 9.5 V (from 10V to 19.5 V)

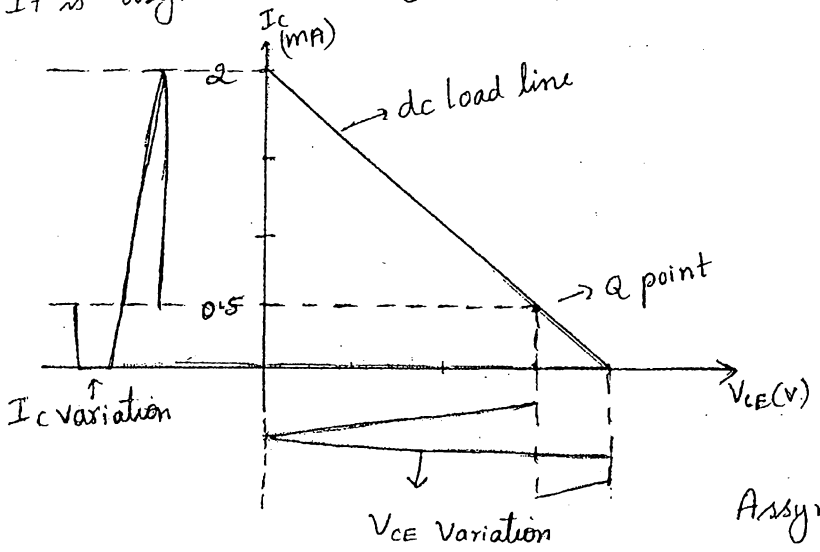
An I_B variation of ±20 μA produces a collector voltage swing of $\Delta V_{CE} = \pm 9.5$ V

* The base current can be varied by smaller amounts.
* The maximum I_C ranges are zero at one extreme and V_{CC}/R_C at another extreme.
* The maximum V_{CE} ranges are zero at one extreme and V_{CC} at another extreme.
* The maximum possible collector voltage swing is approximately ±$V_{CC}/2$.



Q-point selection

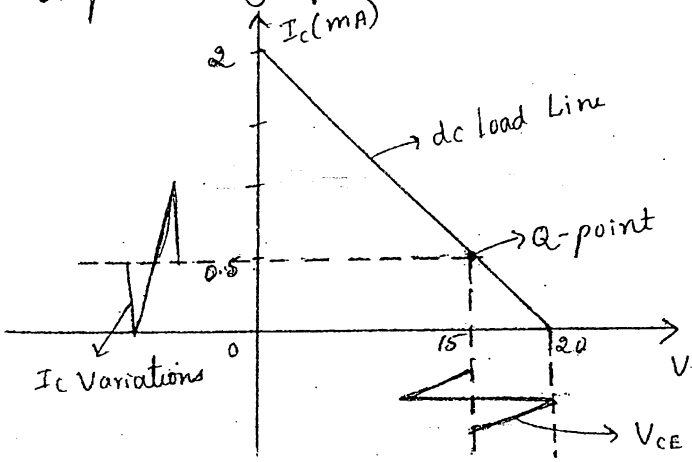
* Consider the previous example, if $I_c = 0.5\ mA$ and $V_{CE} = 15\ V$. Increasing I_c to 2 mA reduces V_{CE} to zero hence $\Delta V_{CE} = -15\ V$. Reducing I_c to zero increases V_{CE} to V_{cc}, produces $\Delta V_{CE} = +5\ V$ It is asymmetric voltage swing.



Assymmetric V_{CE} swing

* When transistor used as an amplifier, the transistor output (Collector emitter) voltage must swing up and down by equal amounts. That is output voltage swing must be symmetrical above and below the bias point.
Hence V_{CE} swing of $-15\ V$ and $+5\ V$ is not suitable.

* If I_c is driven up and down by $\pm 0.5\ mA$ the symmetrical output swing of $\pm 5\ V$ is obtained.



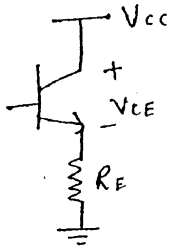
Symmetric ~~variation~~ V_{CE} swing

* In many cases, especially ~~for~~ some large signal amplifiers, circuits are designed to have Q-point at the center of the load line to give the largest possible symmetrical output voltage swing.

Small signal amplifiers usually require voltage swing not greater than ±1V.

Effect of emitter Resistor

* In all examples we considered as R_c as load and have done analysis. If R_E is the dc load. V_{CE} can be written as

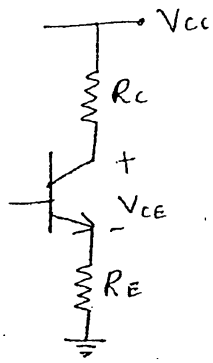


$$V_{CE} = V_{cc} - I_E R_E$$

we consider $I_E \simeq I_c$ and dc load line is drawn exactly as discussed.

$R_L(dc) = R_E$

* If collector and emitter Resistors both present, the total dc Load in series with transistor is $(R_c + R_E)$ then V_{CE} can be written as.



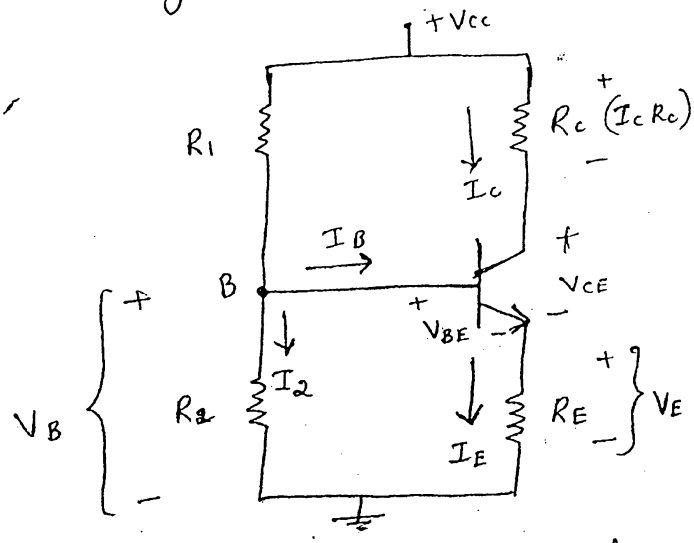
$$V_{CE} = V_{cc} - I_c(R_c) - I_E R_E$$

$$I_C \simeq I_E$$

$$\boxed{V_{CE} = V_{cc} - I_C[R_c + R_E]}$$

Voltage divider bias.

* The voltage divider bias circuit is



* There is an emitter resistor(R_E) along with collector resistor (R_c) in series with transistor. Hence the total dc load in series with transistor is $(R_c + R_E)$

* Resistors R_1 and R_2 constitute a voltage divider that divides the supply voltage to produce base bias voltage.

* Voltage divider bias circuits are normally designed to have the voltage divider current I_2 much larger than base current I_B.

* Refering to above circuit $V_B = \frac{V_{cc} R_2}{R_1 + R_2}$

with V_B constant the voltage across emitter resistor is also a constant quantity

$$V_E = V_B - V_{BE}$$

The emitter current $I_E = \frac{V_B - V_{BE}}{R_E}$

* The collector current [illegible]
as I_E is constant as $I_E = \frac{V_B - V_{BE}}{R_E}$, I_C is held at constant level.

* Refering to above circuit

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_C \approx I_E$$

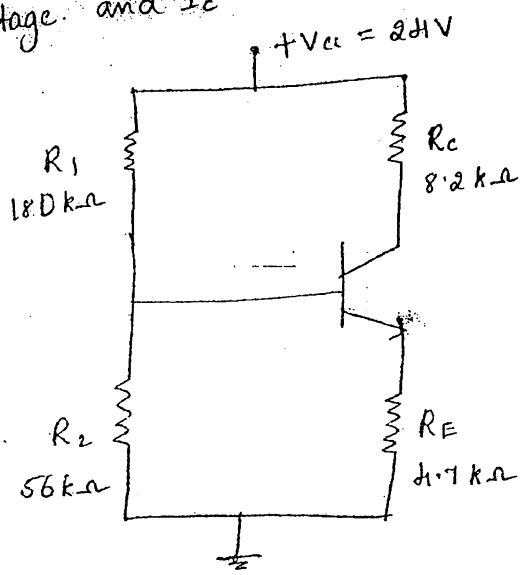
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Transistor h_{FE} is not involved in any of these equations.

Approximate circuit analysis..

Problem

① Analyze the voltage divider bias in circuit in figure to determine the emitter voltage, collector voltage, and collector emitter voltage. and I_C



$$V_B = \frac{V_{cc}\, R_2}{R_1 + R_2} = \frac{24 \times (56\times10^3)}{(56\times10^3) + (180\times10^3)} = 5.69\,V$$

$$V_E = V_B - V_{BE} = 5.69\,V - 0.7\,V \simeq 4.99\,V$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{4.99}{4.7\,k\Omega} = 1.0617\,mA$$

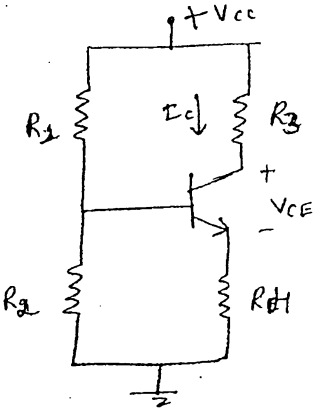
$$I_C \simeq I_E = 1.0617\,mA$$

$$V_{CE} = V_{cc} - I_c\,[R_c + R_E]$$

$$V_{CE} = 24 - 1.0617\,[8.2\times10^3 + 4.7\times10^3]$$

$$V_{CE} = 10.3\,V$$

(2) The voltage divider bias circuit shown in figure has $V_{cc} = 15V$, $R_1 = 6.8\,k\Omega$, $R_2 = 3.3\,k\Omega$ $R_3 = 900\Omega$ $R_4 = 900\Omega$ and $h_{FE} = 50$. Analyze the circuit approximately to determine the levels of I_c and V_{CE}.



$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = 4.9\ V.$$

$$V_E = V_B - V_{BE} = 4.9 - 0.7 = \underline{4.2\ V}$$

$$I_E = \frac{V_B - V_{BE}}{R_{E1}} = \frac{4.2}{900} = \underline{4.666\ mA}$$

$$h_{FE} = \frac{I_C}{I_B}. \quad \alpha = \frac{h_{FE}}{1 + h_{FE}} = \frac{50}{51} = 0.9803$$

$$I_C = \alpha I_{E1} = 0.9803 \times 4.666\ mA = \underline{4.57\ mA}$$

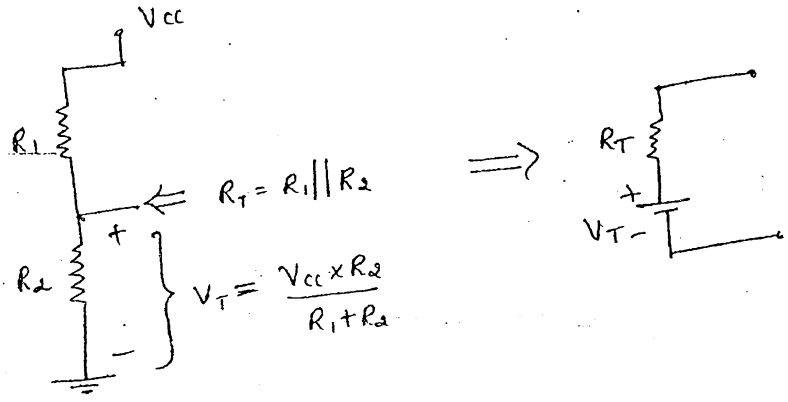
$$V_{CE} = V_{cc} - I_C R_3 - I_E R_{E1}$$

$$V_{CE} = 15 - (4.57 \times 10^{-3})(900) - (4.666 \times 10^{-3})(900)$$

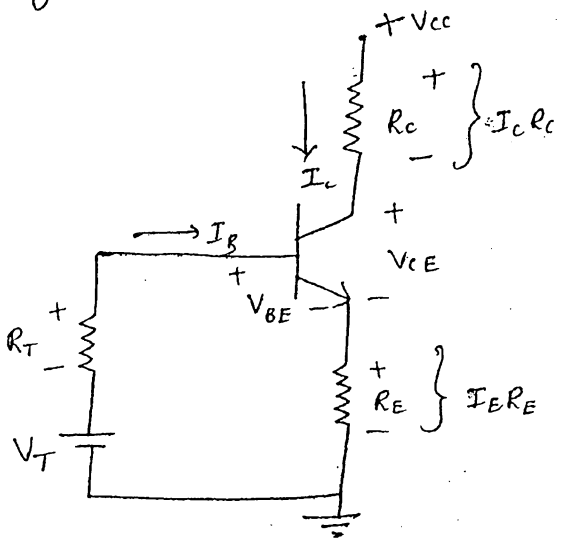
$$\underline{V_{CE} = 6.68\ V.}$$

Accurate Analysis (Precise Circuit Analysis)

* To precisely analyse the voltage divider bias circuit we replace voltage divider by Thevenins equivalent circuit.



Replacing R_T and V_T



$$V_T = \frac{V_{cc} R_2}{R_1 + R_2}$$

$$R_T = R_1 \,||\, R_2$$

From the circuit above, considering voltages around the base emitter circuit

$$V_T = I_B R_T + V_{BE} + R_E (I_B + I_C)$$

$$I_E = I_B + I_C$$

$$I_C = h_{FE} I_B$$

$$V_T = I_B R_T + V_{BE} + R_E I_B (1 + h_{FE})$$

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E (1 + h_{FE})}$$

Once I_B is determined, I_C can be calculated using the appropriate h_{FE} value.

The effects of the maximum and minimum h_{FE} values can also be investigated.

Problem

① Accurately analyze voltage divider biasing circuit, with a supply of 25V, $R_C = 4.7\,k\Omega$, $R_E = 3.3\,k\Omega$, $R_1 = 33\,k\Omega$, $R_2 = 12\,k\Omega$ and $h_{FE} = 50$. Determine the levels of I_C and V_{CE}

$$V_T = \frac{V_{cc} R_2}{R_1 + R_2} = 6.667\ V$$

$$R_T = R_1 || R_2 = 8.8\ k\Omega$$

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E (1 + h_{FE})} = \frac{6.667 - 0.7}{(8.8 \times 10^3) + (3.8 \times 10^3)(1+50)} = 33.69\ \mu A$$

$$I_C = h_{FE} I_B = 50 \times 33.69\ \mu A = \underline{1.684\ mA}$$

$$I_E = I_B + I_C = 1.717\ mA$$

$$V_E = I_E R_E = 5.66\ V$$

$$V_{CE} = V_{cc} - I_C R_c - V_E = 25 - (1.684 \times 10^{-3})(4.7 \times 10^3) -$$

$$\underline{V_{CE} = 11.4852\ V}$$

② A voltage divider bias circuit has $V_{cc} = 15V$, $R_c = 2.7k\Omega$ $R_E = 2.2k\Omega$, $R_1 = 22k\Omega$, $R_2 = 12k\Omega$ Calculate the V_{CE} level

Let's valuate through approximate analysis.

$$V_B = \frac{V_{cc} R_2}{R_1 + R_2} = \frac{15 \times (12 \times 10^3)}{(22 \times 10^3) + (12 \times 10^3)} = 5.294\ V$$

$$V_E = V_B - V_{BE} = 5.294 - 0.7 = 4.594\ V$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{4.594}{2.2 \times 10^3} = 2.088\ mA$$

$$I_C \simeq I_E = 2.088\ mA$$

$$V_{CE} = V_{cc} - I_C R_c - V_E = 15 - (2.7 \times 10^3)(2.088 \times 10^{-3}) - 4.594$$

$$\underline{V_{CE} = \cancel{10.4\ V}\ 4.7684\ V}$$

Voltage divider Bias Circuit design:

* When designing voltage divider bias circuit the voltage divider current (I_2) should be selected much greater than I_1. This makes V_B a stable quantity not much affected by change in h_{FE}

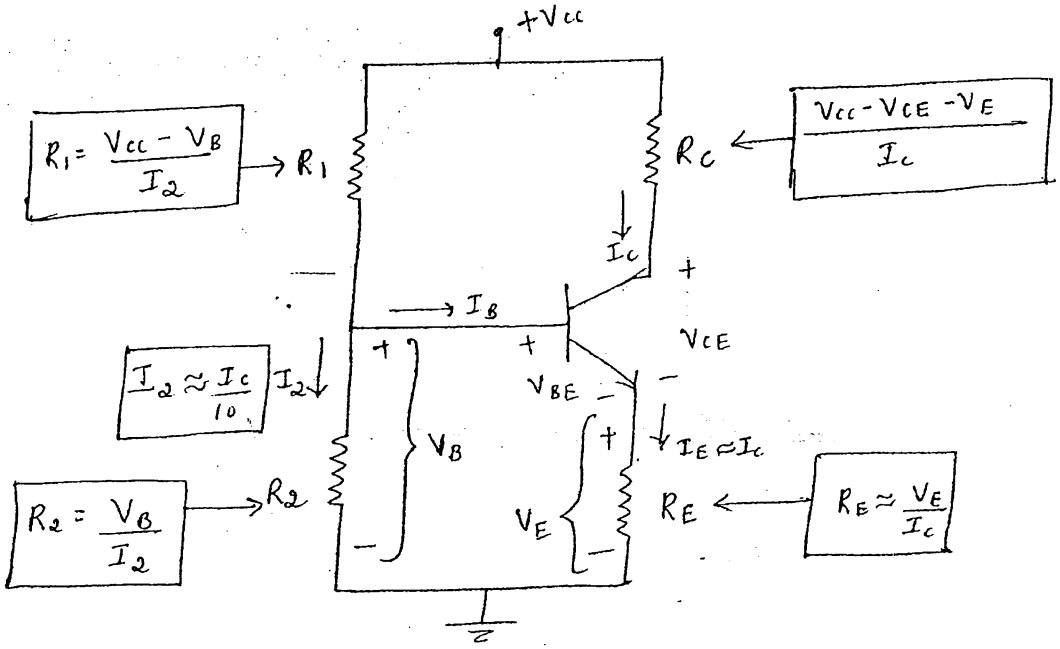
But high level of I_2 results in small resistance values of R_1 and R_2 hence input impedance of the circuit decreases.

* ~~The current I_2~~ If we select current I_2 as

$$I_2 = \frac{I_C}{10}$$

This gives reasonably large values of R_1 and R_2 while still keeping I_2 much larger than I_B.

* V_E should be selected much larger than V_{BE} to give stabilized biasing during variations in temperature and h_{FE}.



Problem

① Design a voltage divider bias circuit to have $V_{CE} = 7V$, $V_E = 6V$ and $I_C = 2mA$. The supply voltage is 20V.

$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_C} = \frac{6}{2\times10^{-3}} = 3\,k\Omega$$

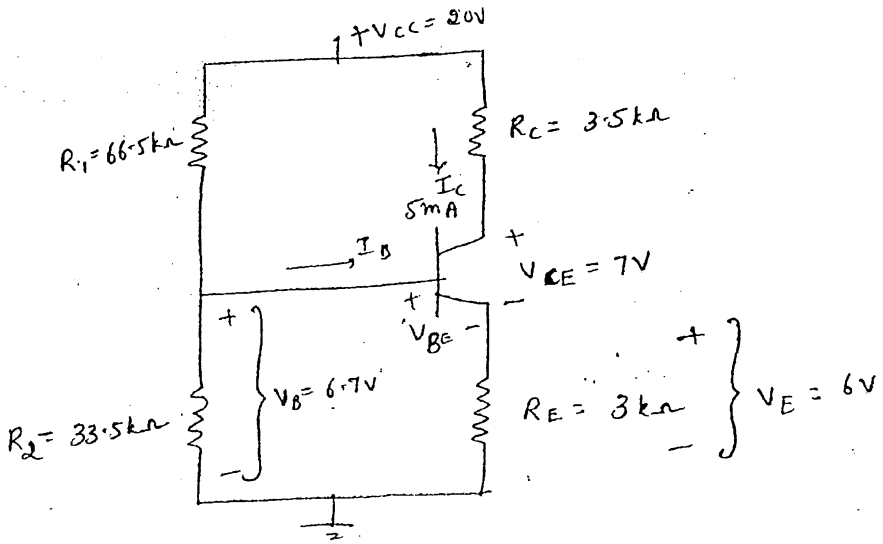
$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20-7-6}{2\times10^{-3}} = 3.5\,k\Omega$$

$$I_2 = \frac{I_C}{10} = \frac{2mA}{10} = \cancel{500\mu A}\ 200\mu A$$

$$V_B = V_E + V_{BE} = 6 + 0.7 = 6.7V$$

$$R_2 = \frac{V_B}{I_2} = \frac{6.7}{200\mu A} = 33.5\,k\Omega$$

$$R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{20-6.7}{200\mu A} = 66.5\,k\Omega$$



Transistors as Switches.

Direct Coupled Switching Circuits.

* Transistor is either biased off to $I_C = 0$, or biased ON to its maximum I_C level.

* In direct coupled switching circuits the signal source will be connected directly to the circuit.

* In figure 1 the negative polarity of the base input voltage V_S biases the transistor off. The current flowing through transistor is only Collector base leakage current (I_{CBO}), as I_{CBO} is so small it can be neglected.

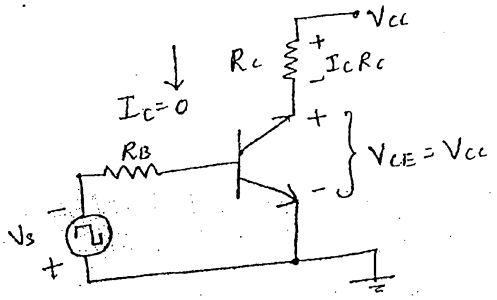


Fig: 1

The transistor collector-emitter voltage is $V_{CE} = V_{cc} - I_C R_C$.

Q_1 is OFF and hence $I_C = 0 \Rightarrow V_{CE} \approx V_{cc}$

* In figure 2, V_S is positive. It biases Q_1 ON to the maximum possible I_C level.

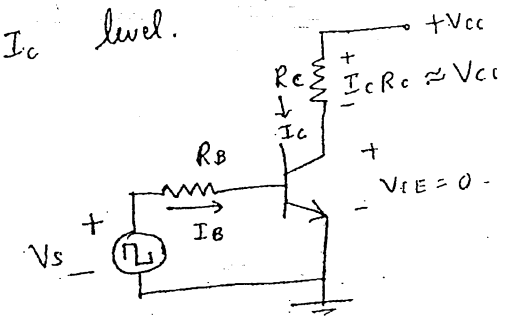


Fig: 2

The collector current is limited only by the collector supply voltage (V_{cc}) and the collector resistor (R_c) Hence

$$I_c R_c \simeq V_{cc} \longrightarrow (1)$$

$$V_{CE} = V_{cc} - I_c R_c \simeq 0 \longrightarrow (2)$$

* The dc load line and output characteristics when $V_{cc} = 10\,V$ and $R_c = 1\,k\Omega$ are shown in fig: 3

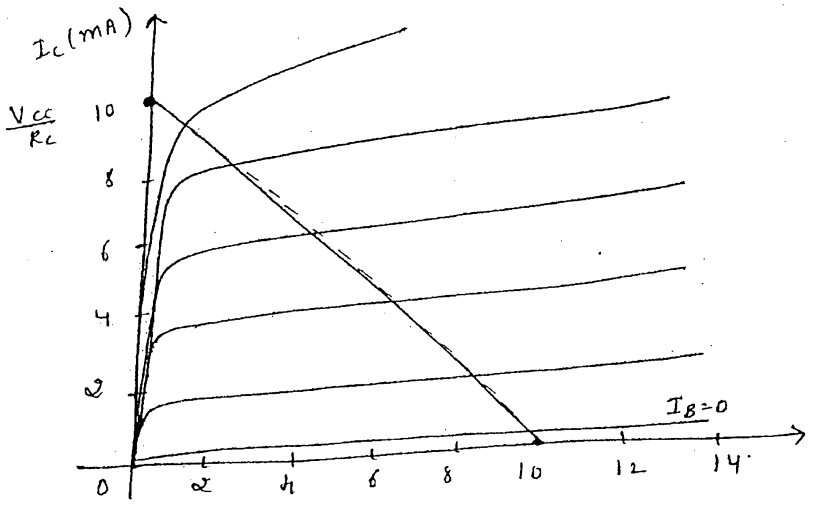


Fig: 3

→ When $I_B = 0$, I_c is close to zero. $I_c = I_{CBO}$, At this point the transistor is said to be cut off. The region below $I_B = 0$ is known as cut off region.

→ when I_c is at its maximum level, the transistor is said to be saturated, and V_{CE} is saturation voltage $V_{CE(sat)}$

$$V_{CE} = V_{CE(sat)}$$

From figure 2, I_B is a constant quantity

$$I_B = \frac{V_s - V_{BE}}{R_B} \longrightarrow (3)$$

The I_c level depends on I_B as

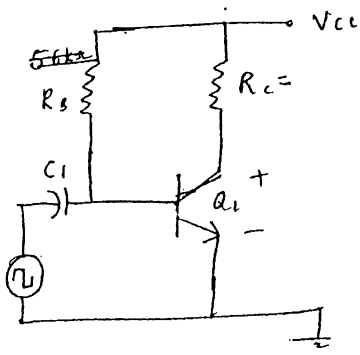
$$I_C = h_{FE} I_B \longrightarrow (4)$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{15}{3.3\,k\Omega} = 4.545\ mA$$

$$I_B = \frac{V_S - V_{BE}}{R_B} = \frac{9 - 0.7}{22\,k\Omega} = 377.27\ \mu A$$

$$h_{FE(1)} = \frac{I_C}{I_B} = 12.047$$

Capacitor Coupled Switching circuit



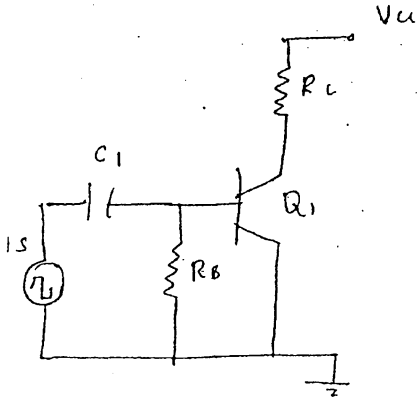
→ This transistor will be ON state with $V_{CE} = V_{CE(sat)}$

→ The capacitor coupled input turns the device off giving $V_{CE} = V_{CC}$

The base current is $I_B = \frac{V_{CC} - V_{BE}}{R_B}$.

The collector current $I_C R_C \approx V_{CC}$

Hence the required h_{FE} value can be calculated.



→ This is another type of capacitor coupled switching circuit.

→ The resistor R_B keeps transistor base-emitter voltage at zero, to ensure that the device is in off state

→ The capacitor coupled input voltage turn the transistor to ON state.

For ON condition of transistor (Saturation), the base current and collector current are calculated using equation ③ & ④ respectively. Then minimum required h_{FE} is

$$h_{FE(1)} = \frac{I_C}{I_B}$$

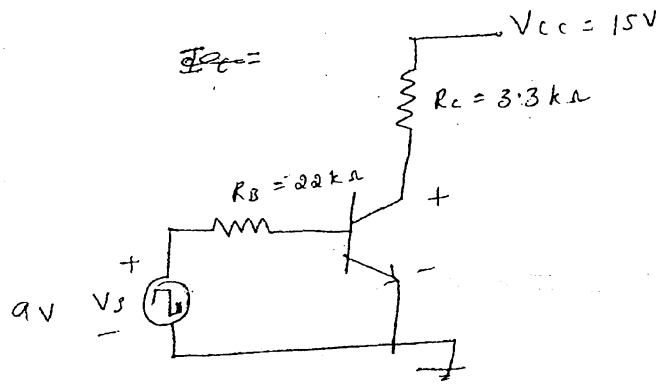
→ If transistor h_{FE} value is less than calculated $h_{FE(1)}$, I_C will be lower than the level required for transistor saturation

→ If $h_{FE} > h_{FE(1)}$, I_C tends to be greater than the current level required for saturation. but it cannot exceed $\frac{V_{CC}}{R_C}$

To ensure that the transistor in switching circuit saturates it must have an h_{FE} value equal to or greater than calculated h_{FE1} for the circuit.

Problem

① A direct coupled transistor switching circuit shown in below figure has $V_{CC} = 15V$, $V_s = 9V$, $R_C = 3.3\,k\Omega$ and $R_B = 22\,k\Omega$. Calculate the minimum h_{FE} for the transistor.



Switching circuit using...

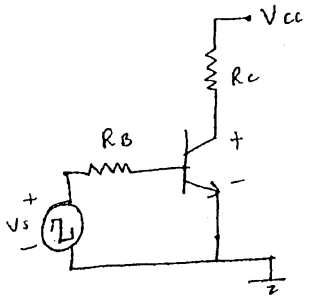
→ The resistance of R_c for any switching circuit can be calculated by using the specified V_{cc} and I_c values using equation

$$R_c \approx \frac{V_{cc}}{I_c}$$

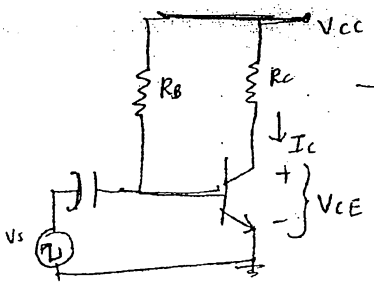
→ ~~$h_{FE(min)}$ value less than 10, will not~~

→ It is very unlikely that transistor will have an $h_{FE(min)}$ value less than 10. Hence we select $h_{FE(min)}$ to be equal to 10. a for calculation of I_B.

→ The value of R_B for different switching circuit can be calculated as.



$$R_B = \frac{V_S - V_{BE}}{I_B}$$

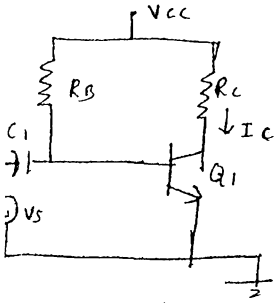


$$R_B = \frac{V_{cc} - V_{BE}}{I_B}$$

→ Typically, the R_B value of 22 kΩ or less is suitable for keeping the transistor biased off.

Problems

① A normally ON capacitor-coupled switching circuit in below figure uses a transistor with $h_{FE(min)} = 25$. The supply voltage is 12V and $R_c = 4.7\,k\Omega$. Determine a suitable resistance for R_B.



$$R_c = \frac{V_{cc}}{I_c} \Rightarrow \qquad I_c = \frac{V_{cc}}{R_c} = \frac{12}{4.7\,k\Omega} = \underline{2.553\ mA}$$

$$I_B = \frac{I_c}{h_{FE(min)}} = \frac{2.553 \times 10^{-3}}{25} = 102.12\ \mu A$$

$$R_B = \frac{V_{cc} - V_{BE}}{I_B} = \frac{12 - 0.7}{102.12\,\mu A} = \underline{110.65\,k\Omega}$$

② A direct coupled transistor switching circuit has $V_{cc} = 5V$ and $V_s = 3V$. Calculate suitable resistance for R_c and R_B to give $I_c = 2.5\ mA$

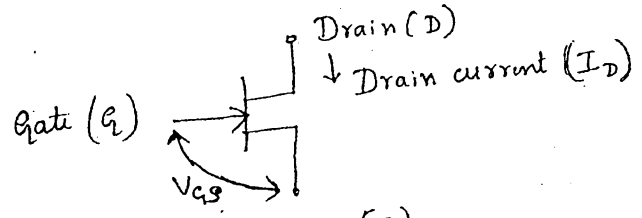
$$R_c = \frac{V_{cc}}{I_c} = \frac{5}{2.5 \times 10^{-3}} = 2\,k\Omega$$

$$I_B = \frac{I_c}{h_{FE(min)}} = \frac{2.5 \times 10^{-3}}{10} = 250\,\mu A$$

$$R_B = \frac{V_s - V_{BE}}{I_B} = \frac{3 - 0.7}{250\,\mu A} = \underline{9.2\,k\Omega}$$

Field Effect Transistor (FET)

→ FET is a three terminal device, Three terminals are Gate (G), Source (S) and Drain (D)



→ Unlike BJT, in FET only one type of charge carriers carry current (majority charge carriers), Hence FET is called unipolar device.

→ FETs are used as switching devices in analog electronic circuits, amplifiers with high input impedance and Integrated circuits (ICs)

The main features of FETs are

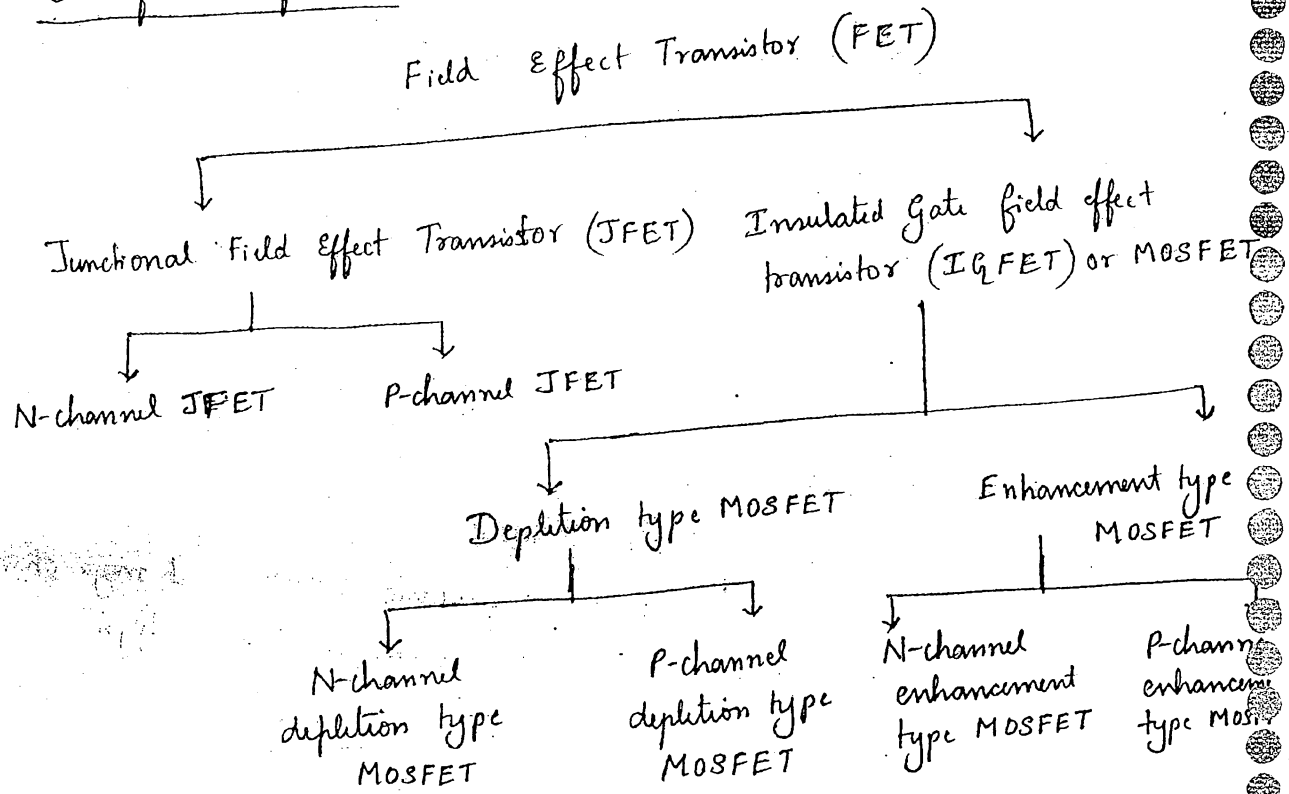
- Ⓐ FETs provide high input impedance, about 1 mega-ohm. Hence FETs are preferred in amplifiers where high input impedance is required.
- Ⓐ The operation of FET depends on the flow of majority carriers only.
- Ⓐ FETs require less space than BJT hence they are used in integrated circuits.

(*) Like BJT, FETs also temperature dependent.
In FET as temperature increases, drain resistance also increases reducing the drain current. Thus unlike BJT, thermal runaway will not occur in FET.
Hence FETs are more stable than BJT.

(*) The noise in FET is relatively small with respect to BJT

(*) It has zero offset voltage at zero drain current.

Classification of FET



and insulated gate field effect transistor (IGFET) or Metal-oxide Semiconductor FET (MOSFET)

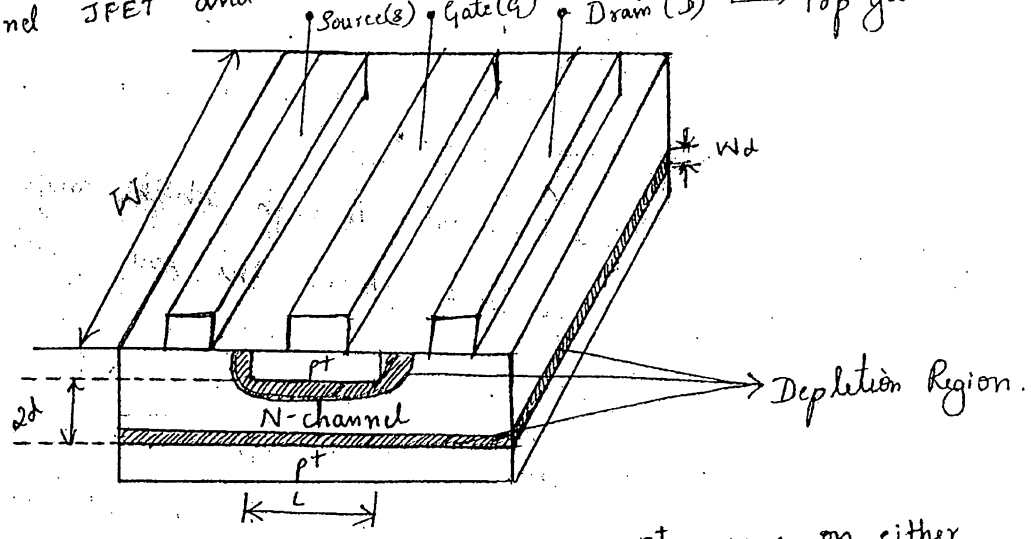
→ Depending on type of channel, JFET can be further classified as N-channel and p-channel J-FET

→ Depending on operating principle of MOSFET, it is classified as depletion type MOSFET and enhancement-type MOSFET. Again MOSFET is classified as N-channel and P-channel MOSFET

Junction Field Effect Transistor. (JFET)

→ JFET has a conducting channel with ohmic contacts on either end. Channel will be either N-type or P-type.
Depending on types of channel JFET can be classified as N-channel JFET and P-channel JFET.

Figure: 1



→ In structure of JFET, there are two p^+ regions on either side of N-channel. p^+ Region is heavily doped region. This forms two p^+N -junctions.

→ Two P^+ regions are [illegible] output terminal is available from the device and it is called gate terminal (G).

→ One side of ohmic contact of channel is called Source (S) and other side is known as Drain (D)
The electrons enter through the source terminal (S) and exit through drain (D)

→ Simplified representation

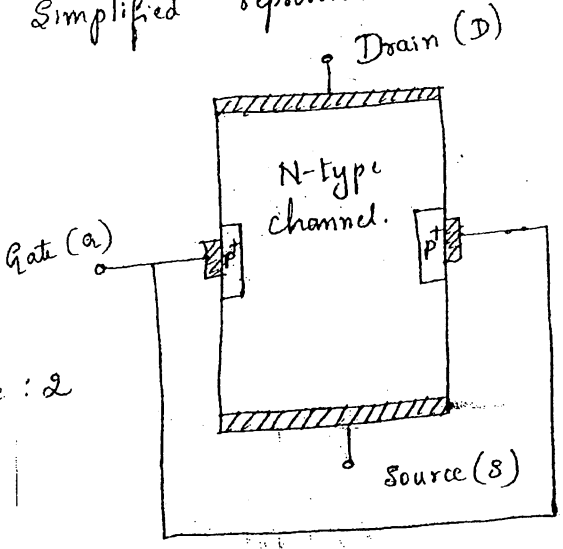
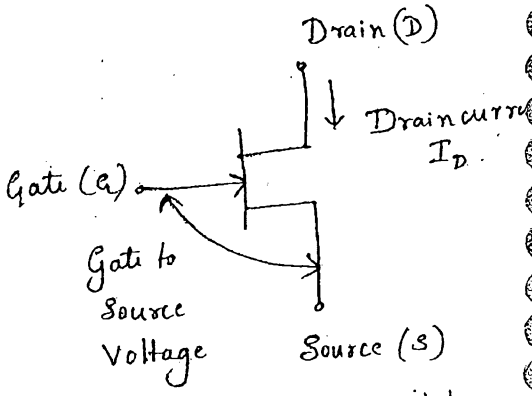


Figure : 2



N-channel JFET and circuit Symbol.

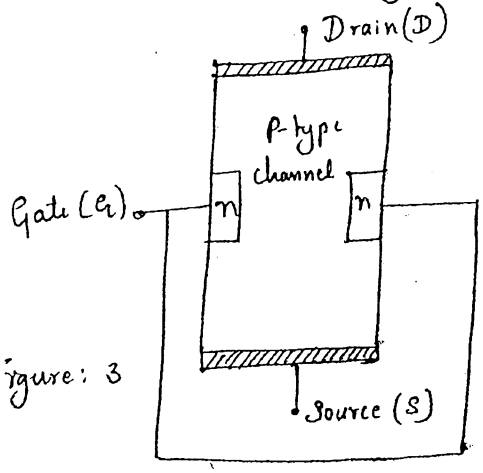
1. Source (S) : The terminal through which majority carriers can enter into semiconductor bar. The source current is indicated as I_S.

2. Drain (D) : The terminal through which majority charge carriers exit out of the device. The current entring to the semiconductor through drain terminal is designated as I_D. The voltage between drain and source is indicated as V_{DS}.

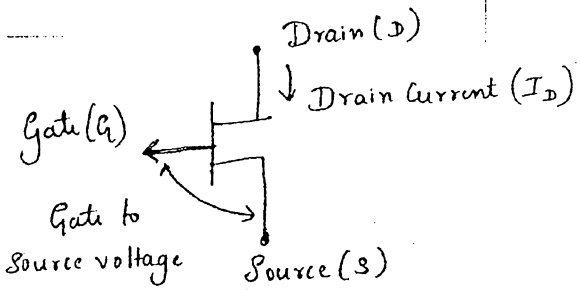
regions on either side of the N-channel.

The voltage between gate and source is called V_{GS}. The V_{GS} is applied in the direction to the reverse bias of PN junction.

The current entering through Gate terminal is represented as I_G.



igure: 3



P- channel JFET and circuit symbol

→ In an N-channel JFET, if p^+N-junction is reverse biased, electrons and holes diffuse across the junction and leaves positive ions on N-side and negative ions on P-side.
These ~~immobile~~ positive and negative ions are immobile and forms depletion region.

→ Since P side ~~is~~ heavily doped, the depletion region extends more into N-channel in N-channel JFET.
In P-channel JFET since n side is heavily doped the depletion region extends more into P-channel.

→ The depletion region when p^+N junction is reverse biased ~~through~~ by applying reverse potential to gate and Source terminal can be shown ~~as~~ in Figure 4.

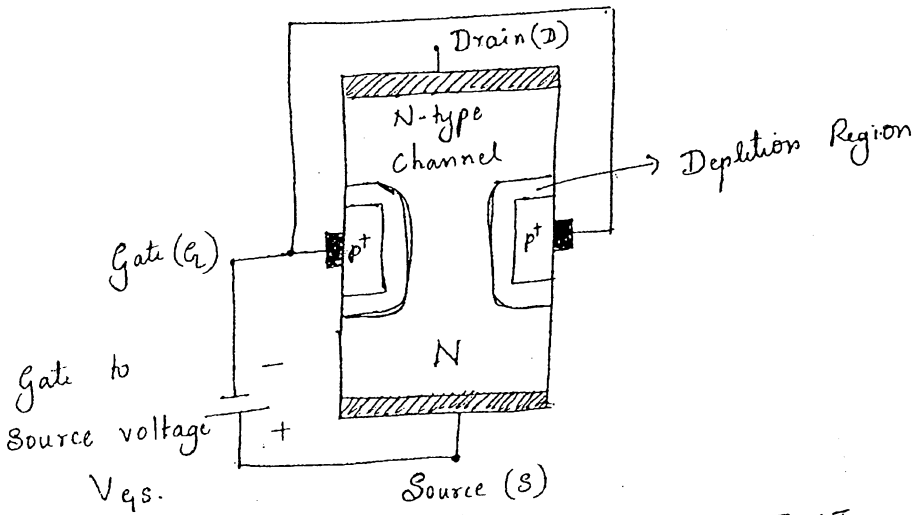


Figure: 4 Depletion region in N-channel JFET

→ By varying the V_{GS} the width of the channel can be controlled. with the increase in reverse bias voltage V_{GS}, the depletion region increases in N-type channel hence channel width reduces.

When the voltage ~~becomes~~ between gate and source ~~voltage~~ becomes zero all of a sudden, the depletion region reduces and hence channel width increases.

→ The gate to source p^+N-junction of a JFET can be reverse biased when the drain is connected to the positive terminal of the dc supply (V_{DD}) and source is connected to the negative terminal of dc supply. and gate is open.

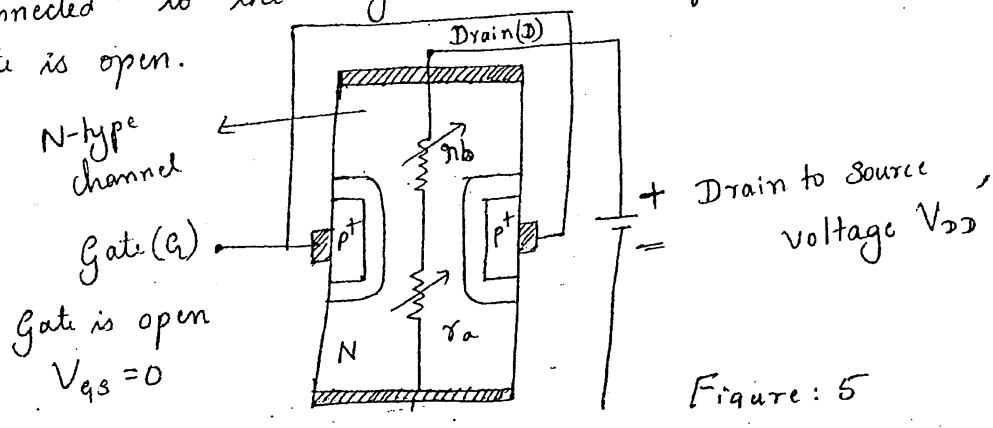


Figure: 5

→ Here r_a and r_b are channel [illegible]

variable. Its ~~value~~ ~~do~~ Values of r_a and r_b depends on the magnitude of gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}).

→ When gate (G) terminal is opened and V_{DD} is applied across drain to source, electrons flow from source to drain through N-type channel. As a result drain current (I_D) flows from drain to source.

Due to drain current, there will be voltage drop across the resistance r_b. This voltage across r_b provides the effect of reverse biasing of the gate to source P^+N junction. When the gate is open, the gate to source P^+N junction is reverse biased by drain to source voltage. The developed depletion region within the device can be shown below.

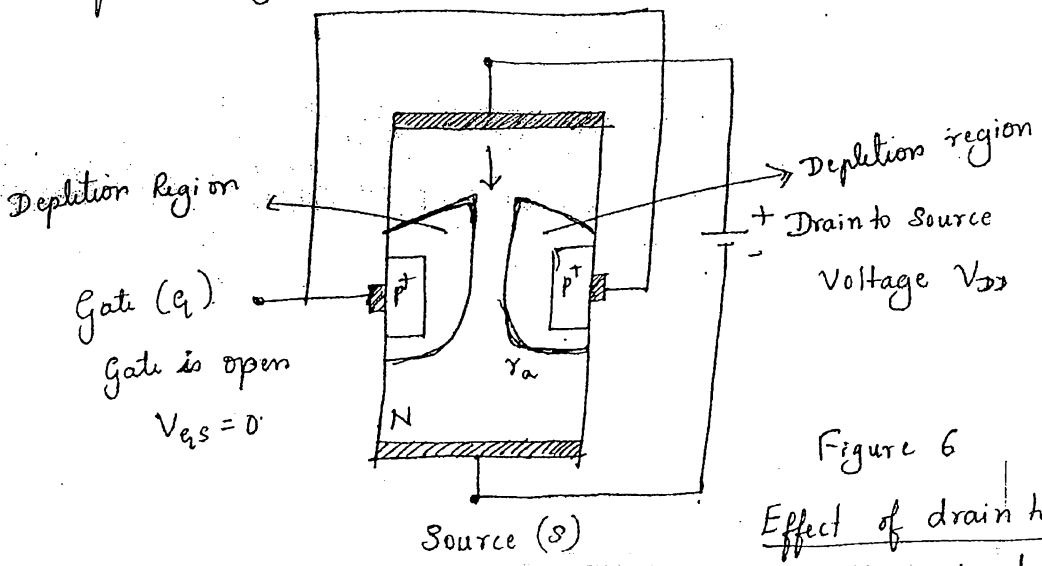


Figure 6

Effect of drain to source voltage in depletion Region.

→ The depletion region is extended deeper in the N-channel near the drain terminal. The thickness of depletion region is less near source

→ The voltage across n_b is greater than [illegible]. ... reverse bias voltage is comparitively high near drain with respect to source.

Operation of JFET

→ Below figure:7 shows an N-channel JFET schematic block diagram.

The channel length is L and depth 2d. The depletion region width is W_d.

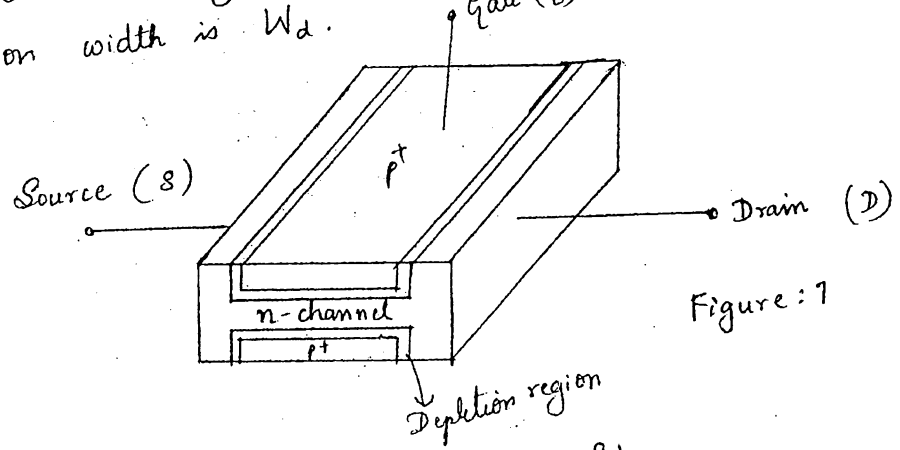


Figure: 7

The channel resistance is $R = \frac{\rho L}{A}$

ρ → Resistivity of the channel. (Ω/m)

σ is the reciprocal of ~~conductivity~~ Resistivity. (mho/m)

$$\sigma = 1/\rho$$

Hence $$R = \frac{\rho L}{A} = \frac{L}{\sigma A} \longrightarrow (1)$$

$$\sigma = e \mu_n N_D \longrightarrow (2)$$

e → magnitude of electric charge.

μ_n → Mobility of electrons

N_D → Donor Concentration

The effective cross sectional area of channel is

$$A = \text{Area of channel} - \text{Area of depletion region}$$

$$A = (W)(2d) - (W)(2W_d)$$

$$A = 2W(d - W_d) \longrightarrow (3)$$

Substituting eqn (2) & (3) in (1)

$$R = \frac{L}{2e\mu_n N_D W (d - W_d)}$$

Schematic diagram of an N-channel JFET can be shown as

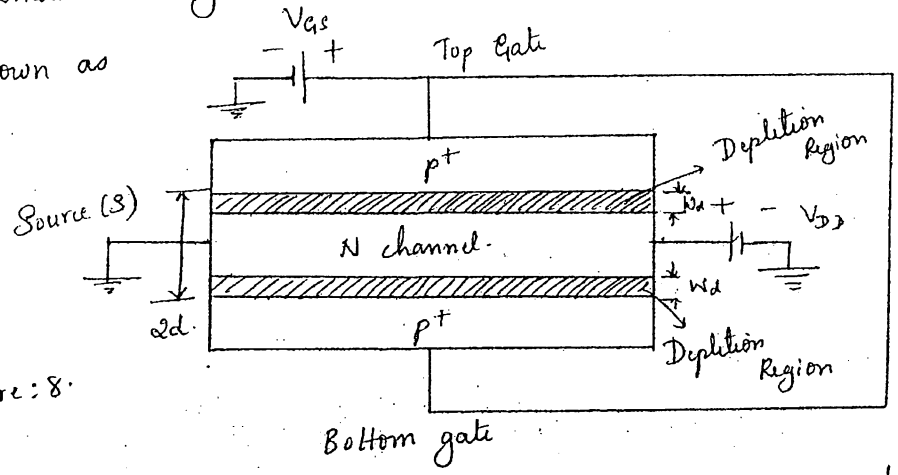


Figure: 8.

→ If gate to source voltage $V_{GS} = 0$ and drain to source voltage V_{DS} is very small value (about zero) the reverse bias across p^+N junction is constant and the thickness of the depletion region across the p^+N junction is uniform. as shown in figure 8

→ If Drain to Source voltage $V_{DS} = 0$ and gate to source voltage V_{GS} decreases from zero, the reverse bias across progressively from source to drain

Consequently the depletion
channel width is reduced from source to drain. If again the V_{GS} decreases, the thickness of depletion region increases. until the two depletion region may contact each other. At this V_{GS} the channel may cut off completely, hence this value of V_{GS} is known as cut-off voltage.

→ When $V_{GS}=0$ and voltage V_{DS} increases gradually from zero, the drain is positive with respect to source. Then majority charge carriers (electrons) can flow from source to drain through N-type channel. The drain current I_D flows from drain to source.

The magnitude of drain current depends on

1. The majority carriers available in the channel (N-type)
2. The resistance of channel, which depends on
   - * Length of channel L
   - * Cross sectional area of channel i.e. $A = 2W(d - W_d)$
3. The magnitude of applied voltage V_{DS}

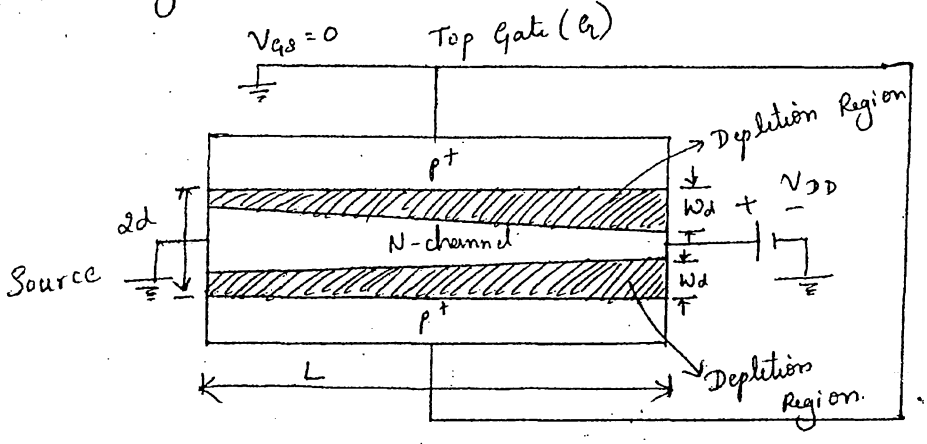


Figure : 9

→* Due to the resistance of the channel and V_{DS}, the positive potential is gradually increased from source to drain. (Drain will be at higher positive potential than Source).

Therefore, the reverse voltage across the P^+N - junction increases and width of the depletion region also increases as shown in figure 9

→ With increase in the voltage V_{DS}, the effective channel cross sectional area decreases. As a result channel resistance increases and rate of change of drain current I_D decreases with increase in V_{DS}.

Hence the output characteristics shows some linear characteristics. This can be shown in figure 10

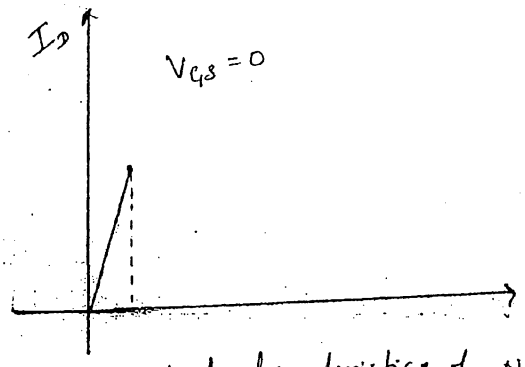


Figure : 10

Output characteristics of N-channel JFET, $V_{GS} = 0$ $V_{DD} > 0$ in linear zone

→ When the voltage V_{DS} is further increased progressively, the cross sectional area will be reduced. At a certain value of V_{DS}, the cross-sectional area of the channel becomes zero and the channel will be pinched off P; as shown in figure 11

The drain voltage at which pinch off occurs is called pinch-off voltage represented by V_P.

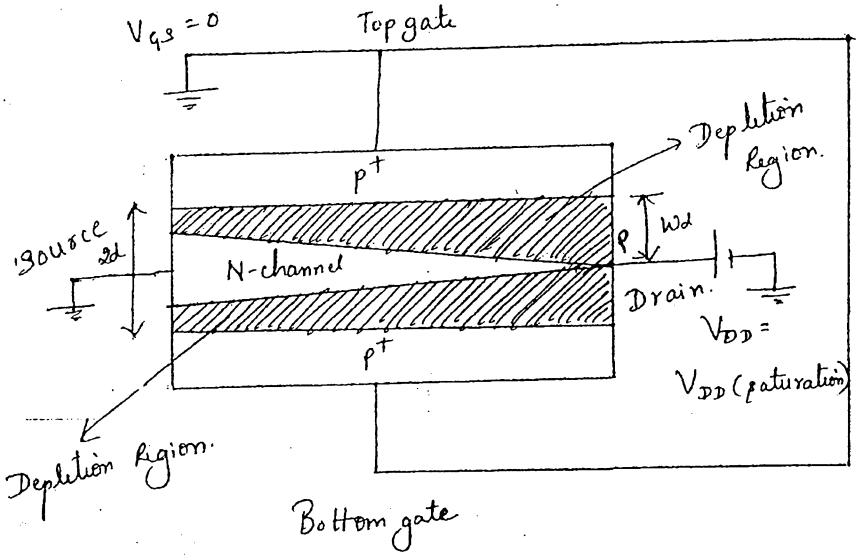


Figure : 11

→ As the depletion region width increases with increasing V_{DS} at a certain value of V_{DS} the two depletion regions touch each other. At that time, the depletion region width (W_d) is equal to d at the drain and this is represented by the pinch-off point P as shown in figure. 11.

At pinch off point, the drain current is designated by $I_{D(saturation)}$ and drain to source voltage is represented by $V_{DS(saturation)}$ The output characteristics of JFET up to the pinch-off point is shown figure. 12

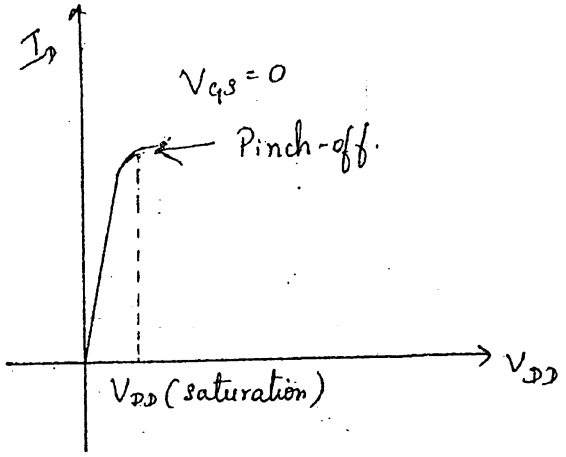


Figure : 12

→ When V_{DS} further increased the pinch off point shifts towards source terminal as shown in figure 13. The voltage drop in the channel between the source and pinch-off point is constant. The constant drain current (I_D) flows after the pinch-off point as dipicted in Figure 14 and device operates in saturation region.

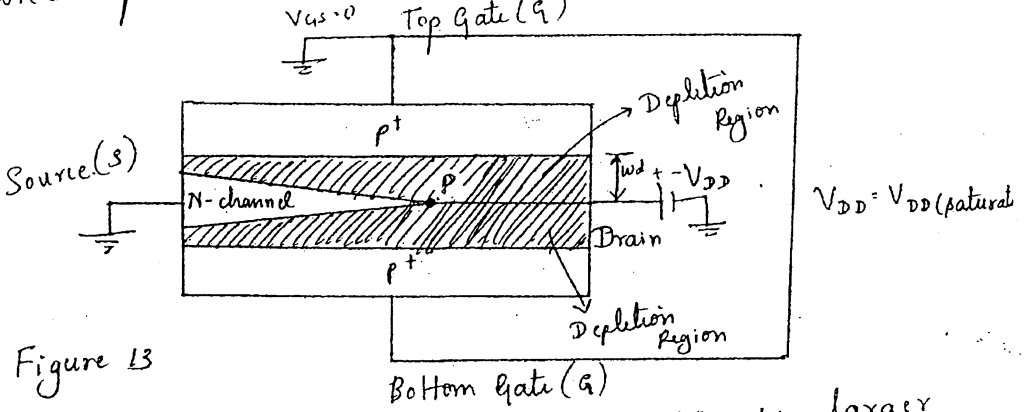


Figure 13

When $V_{GS} < 0$, the depletion region width W_d is larger than the depletion region width with $V_{GS} = 0$. Then the cross-sectional area of the channel is reduced as shown in figure 15, and the resistance value will be increased. The drain current is reduced for any value of V_{DS}

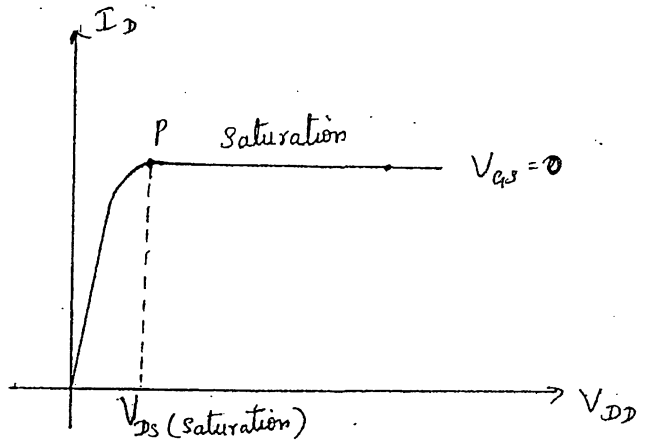


Figure. 14

Output characteristics of N-channel JFET with $V_{GS}=0$

~~For~~

If V_{DS} is increased gradually with $V_{GS} < 0$, the different output characteristic curve will be obtained. This output characteristics of the JFET for different values of V_{GS} are depicted in figure. 16

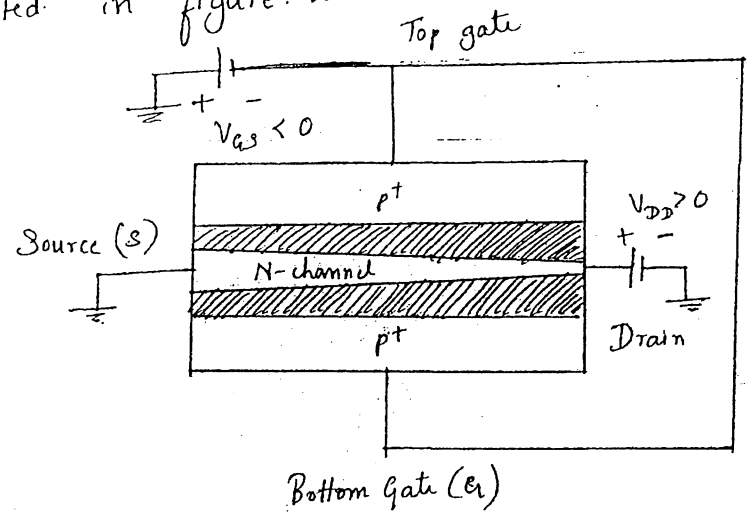


Figure 15

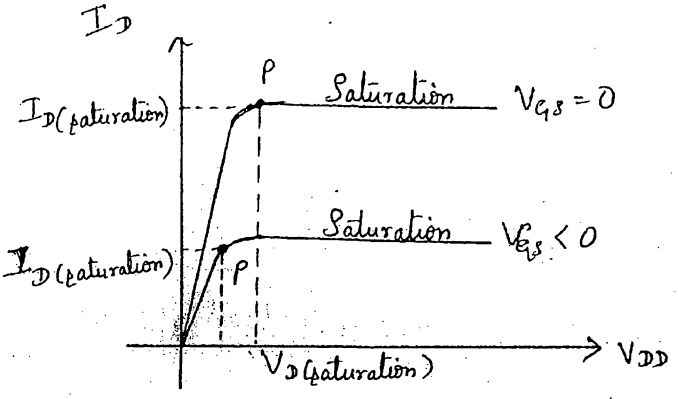


Figure 16.

Output characteristics of N-channel JFET with $V_{GS} = 0$ and $V_{DD} > 0$ and $V_{GS} < 0$ and $V_{DD} > 0$.

Characteristics

→ Set of curves which represents the relationship between current and voltages.

→ JFET has two important characteristics. → Drain characteristics
→ Transfer Characteristics.

Drain Characteristics.

→ Family of curves which relates between the drain current (I_D) and drain to Source voltage (V_{DS}) for different values of gate to Source voltage (V_{GS})

→ Figure 17 shows the circuit diagram of JFET to determine drain characteristics of JFET. The potentiometer (P_1) is used to vary the gate to Source voltage V_{GS} and potentiometer P_2 is used to vary the drain to Source voltage V_{DS}. The V_{GS} and V_{DS} voltages are measured by voltmeters and drain current (I_D) can be measured by milli-ammeter.

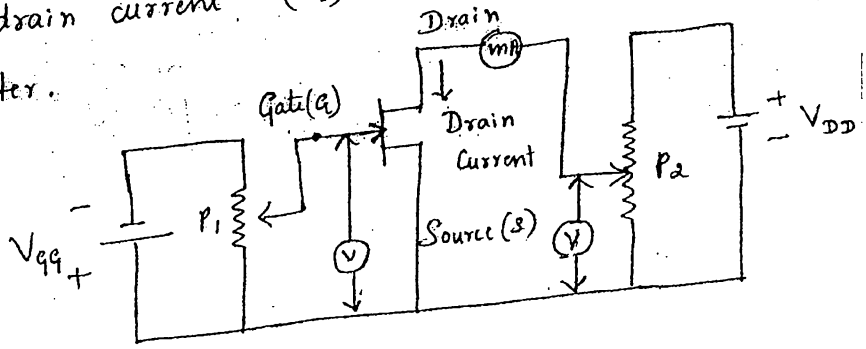


Figure 17
Circuit diagram of an N-channel JFET to obtain characteristics. (Drain and Transfer characteristics)

→ To get drain characteristics initially we maintain $V_{GS} = 0V$ and then increase the drain to source voltage V_{DS} in small steps and measure the drain current in each step of V_{DS}.

Then the characteristic curve with drain to source voltage (V_{DS}) and drain current (I_D) are plotted.

→ There are three regions in characteristic curve

1. Linear Region
2. Saturation (pinch-off) Region
3. Breakdown Region.

Linear Region: In this region, the drain current (I_D) increases linearly when the drain to source voltage V_{DS} increases linearly and it flows according to Ohm's law.

In figure 18 the, the region OA is linear Region.

In this region N-channel acts as a resistance

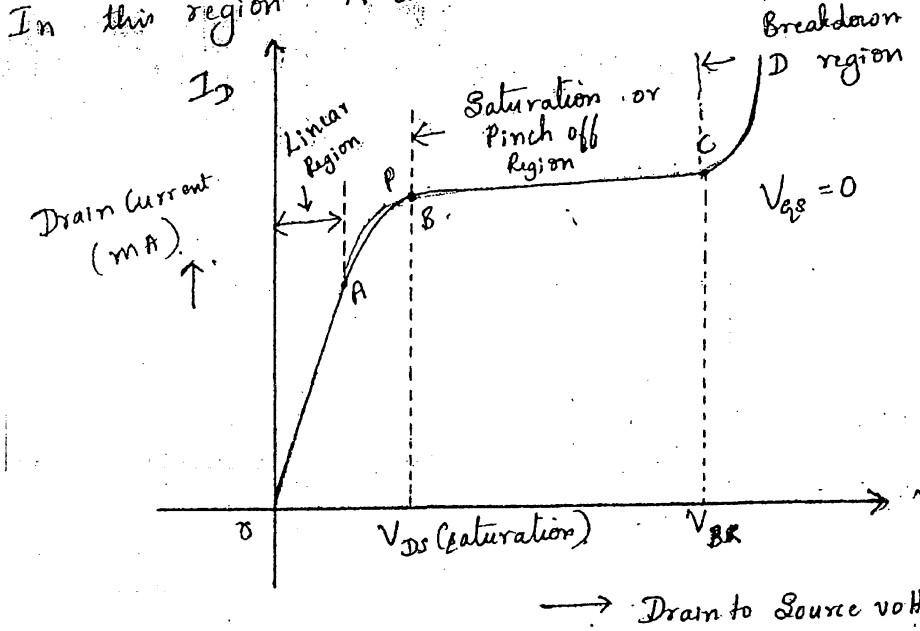


Figure 18

→ The region BC in figure is ~~km~~ called saturation region. Since the drain current (I_D) remains constant at its maximum value (I_{DSS}) this region is also called constant current region.

The drain current in saturation region is

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

I_{DSS} → Drain Saturation current

V_{GS} → Gate to Source voltage

V_P → Pinch off voltage.

Above equation is known as Shockley's equation

→ Usually JFET is used as an amplifier when it operates in pinch-off region.

→ Consider the schematic diagram of a FET when Gate to Source voltage is $-V_{GS}$ and drain to source voltage is V_{DD}, ~~As~~ as ~~shown~~ in figure 19

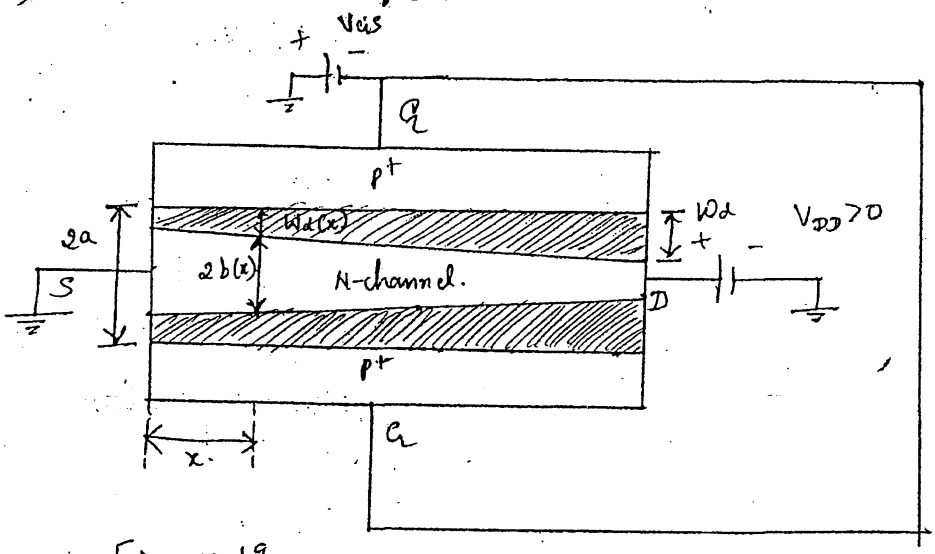


Figure 19

→ Assume p^+ region is doped with N_A acceptors / cubic metre and N region is doped with N_D donors per cubic metre

The p^+N junction is not uniform.

$N_A \gg N_D$, $w_n \gg w_p$

The space charge width is $w_n(x) = w_d(x)$

$$w_d(x) = a - b(x) = \left[\frac{2\varepsilon}{qN_D}\{V_0 - V(x)\}\right]^{1/2} \longrightarrow (a)$$

$\varepsilon \rightarrow$ Dielectric constant of channel material

$q \rightarrow$ Magnitude of charge of electron

$V_0 \rightarrow$ Junctioned contact potential at distance x.

$V(x) \rightarrow$ The applied potential across space charge region at a distance x., it is negative for applied reverse bias.

At pinch off condition, $b(x)$ is zero and $w_d(x) = a$

$V \gg V_0$, Assume $V(x) = V_p$., and from equation (a)

$$|V_p| = \frac{qN_D}{2\varepsilon} a^2 \longrightarrow (b)$$

when $V_0 - V(x)$ is represented by V_{GS}

$$a - b(x) = \left[\frac{2\varepsilon}{qN_D} V_{GS}\right]^{1/2}$$

$$V_{GS} = \frac{qN_D}{2\varepsilon}\{a - b(x)\}^2$$

$$= \frac{qN_D}{2\varepsilon} a^2 \left[1 - \frac{b(x)}{a}\right]^2$$

$$V_{GS} = V_p \left[1 - \frac{b(x)}{a}\right]^2$$

$\frac{1}{V_p} = \left[\frac{1}{a}\right]$

From above equation we get $b(x) = a\left[1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}\right]$ → (d)

Breakdown Region.

→ When drain to source voltage is increased above V_{BR}, the drain current I_D increases rapidly ~~hence the drain current~~.

At this potential, breakdown of gate to source junction occurs due to avalanche effect.

This region is represented by CD in figure 18

→ When the gate to source voltage reduces from zero, the value of pinch off voltage will be smaller than pinch off voltage at $V_{GS} = 0$

Figure 21 and 22 show the circuit diagram of P-channel JFET and Drain characteristics of P-channel JFET.

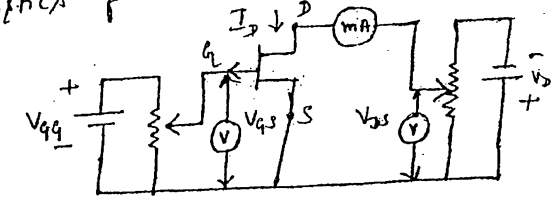


Figure 21

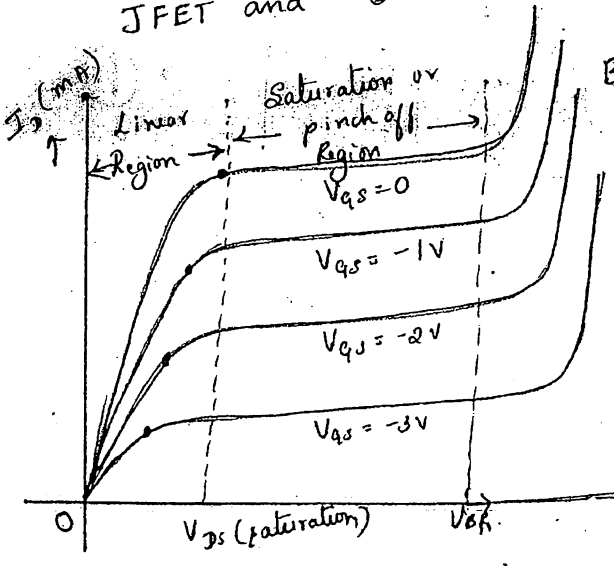
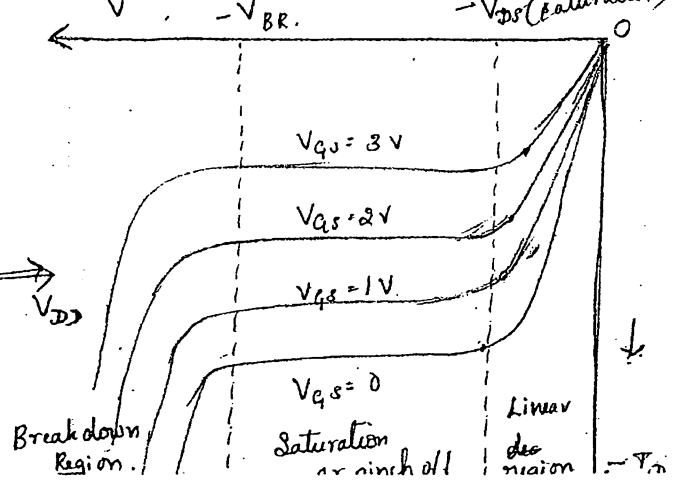


Figure 22



Transfer Characteristics

→ It is the relationship between drain current I_D and gate to source voltage V_{GS} for constant values of V_{DS}.

→ In figure initially V_{DS} is maintained at specified value the V_{GS} is increased in small steps and the corresponding drain current at each step is measured and plotted.

→ Figure shows transfer characteristics, the nature of this curve is parabola

$$i_D = i_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = i_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \longrightarrow (e)$$

i_D → Drain current

i_{DSS} → Saturation drain current when $V_{GS} = 0$

$V_{GS(off)}$ → V_P is the pinch-off voltage.

Differentiating equation (e) with respect to V_{GS}

$$\frac{\partial i_D}{\partial V_{GS}} = i_{DSS} \times 2\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{-1}{V_P}\right] \longrightarrow (f)$$

$\frac{\partial i_D}{\partial V_{GS}} = g_m$ at constant V_{DS} → Transconductance (mho)

$$g_m = \frac{-2 i_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] \longrightarrow (g)$$

From equation (e)

$$\left[1 - \frac{V_{GS}}{V_P}\right] = \left[\frac{i_D}{i_{DSS}}\right]^{1/2} \longrightarrow (h)$$

By substituting value of $\left[\frac{V_{GS}}{V_P}\right]$

using equation (9)

$$\frac{g_m V_P}{(-2 I_{DSS})} = \left[\frac{i_D}{I_{DSS}}\right]^{1/2}$$

$$g_m = \frac{-2\sqrt{i_D I_{DSS}}}{V_P}$$

at $V_{GS}=0$, $g_m = \frac{-2 I_{DSS}}{V_P} \Rightarrow g_{mo} = \frac{-2 I_{DSS}}{V_P}$.

→ The slope of transfer characteristics at drain current I_{DSS} is

$$g_m = \frac{-2\sqrt{i_D I_{DSS}}}{V_P}$$

$$\frac{\partial i_D}{\partial V_{GS}} = \frac{-2\sqrt{i_D I_{DSS}}}{V_P}$$

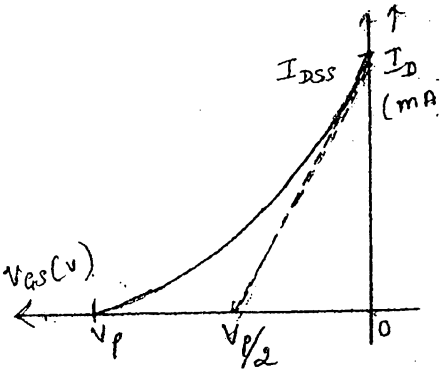


Figure 23.

at $i_D = I_{DSS}$, $\frac{\partial i_D}{\partial V_{GS}} = \frac{-2 I_{DSS}}{V_P} = \frac{I_{DSS}}{-V_P/2}$.

When a trangent is drawn at $i_D = I_{DSS}$ and $V_{GS}=0$ the characteristic curve can intercept at $-V_P/2$ on x-axis. as shown in figure. 23

The gate to source cut-off voltage is also equal to pinch-off voltage V_P hence

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2.$$

Characteristic Parameters of JFET

→ The drain current i_D of JFET is a function of V_{GS} and V_{DS}

$$i_D = f(V_{GS}, V_{DS})$$

When any of V_{GS} and V_{DS} is fixed, the relationship between other two variables can be used to determine the following three parameters.

- (*) Transconductance (g_m)
- (*) Drain Resistance (r_d)
- (*) Amplification factor (μ)

From Taylor series expansion., the change in drain current can be represented by

$$\Delta i_D = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} \Delta V_{GS} + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_{V_{GS}} \Delta V_{DS}$$

① Transconductance (g_m): It is the slope of transfer characteristics of curves.

$$g_m = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} = \frac{\Delta i_D}{\Delta V_{GS}} \quad \text{when } V_{DS} \text{ is constant}$$

g_m is also known as mutual conductance.

Its unit is mho.

It can be defined as ~~small change in~~ ratio of small change in drain current to corresponding small change in gate to source voltage i.e, $\frac{\Delta i_D}{\Delta V_{GS}}$ when V_{DS} is constant.

drain characteriptice is called drain resistance and it is defined as

$$r_d = \left.\frac{\partial V_{DS}}{\partial i_D}\right|_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta i_D}$$ where V_{GS} is constant

r_d is the ratio of a small change in the drain ~~current~~ voltage ΔV_{DS} to the corresponding small change in drain current Δi_D when gate voltage V_{GS} held constant.

3) Amplification factor (μ)

The amplification of JFET is defined as

$$\mu = -\left.\frac{\partial V_{DS}}{\partial V_{GS}}\right|_{I_D} = -\frac{\Delta V_{DS}}{\Delta V_{GS}}$$ when I_D is constant

The ratio of small change in drain voltage ΔV_{DS} to small change in ~~drain~~ source voltage ~~when~~ ΔV_{GS} when drain current is constant.

The negative sign represents that when V_{GS} increased, V_{DS} will be decreased. at constant drain current I_D.

we know the equation of change of drain current

$$\Delta i_D = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} \Delta V_{GS} + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_{V_{GS}} \Delta V_{DS}$$

divide both side by ΔV_{GS}

$$\frac{\Delta i_D}{\Delta V_{GS}} = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_{V_{GS}} \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Since i_D is constant $\frac{\Delta i_D}{\Delta V_{GS}} = 0$.

$$0 = \frac{\partial i_D}{\partial V_{GS}}\bigg|_{V_{DS}} + \frac{\partial i_D}{\partial V_{DS}}\bigg|_{V_{GS}} \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Substituting the value of the partial differential coefficients -

$$0 = g_m + \left(\frac{1}{r_d}\right)(-\mu)$$

$$\boxed{\mu = r_d g_m}$$

∴ Amplification factor is the product of drain resistance (r_d) and transconductance (g_m)

Comparison between FET and BJT

FET

1. FET is unipolar device as current flows through device due to either electrons or holes
2. FET is voltage controlled device
3. Input impedance is very high. ($M\Omega$)
4. FET has negative temperature coefficient. The current decreases with increase in temperature
5. Since minority charge carrier effects do not exists in FET this device operates at high switching speed and

BJT

1. BJT is bipolar device as current flows through device due to both electrons and holes.
2. Current controlled device.
3. Input impedance is less ($k\Omega$)
4. The device has positive temperature coefficient. The current increases with increase in temperature.
5. ~~Since~~ Because of minority charge carrier effect, the device operates at low switching speed and cut-off frequency.

⑥ FET has less noise when compared to BJT, these are used in amplifiers and low level signals.

⑦ FET occupies less space compared to BJT hence these used in fabrication of IC.

Compared to FET

⑦ BJT requires more space to fabricate IC when compared to FET.

MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

→ * Aluminium Metal is used in MOSFET.

The oxide layer consists of SiO_2 and its thickness is given by t_{oxide}.

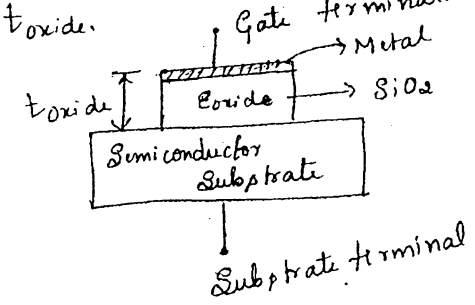


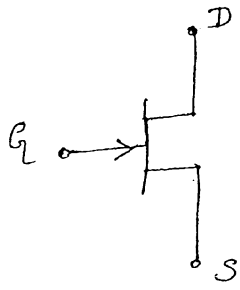
Figure 24

ϵ_{oxide} is the oxide permittivity

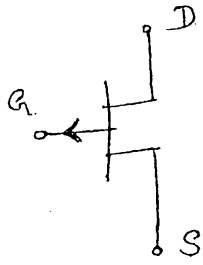
Advantages of MOSFET

* It requires very small area on an Integrated Circuit (IC)
* Digital circuits can be designed using only MOSFET.
* High density VLSI circuits such as microprocessors, microcontrollers and memory ICs can be designed using MOSFET.
* MOSFET can be used in analog circuits as switching devices and amplifiers.

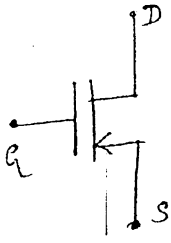
Circuit symbols of ...

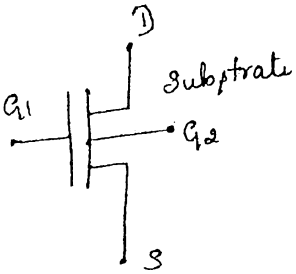


N-channel JFET

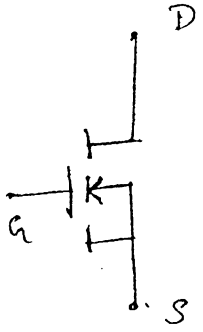


P-channel JFET

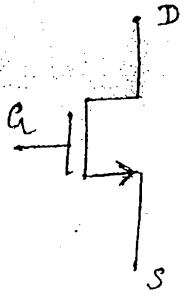


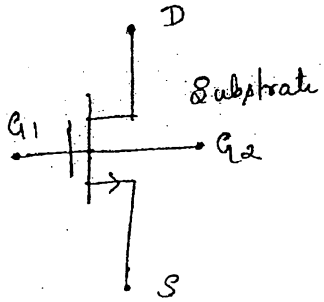


N-channel depletion or enhancement type MOSFET

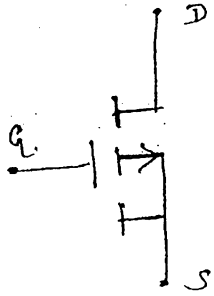


N-channel Enhancement type MOSFET.





P-channel depletion or enhancement type MOSFET



P-channel enhancement type MOSFET.

B.E III SEMESTER DECEMBER 2013/JANUARY 2014 EXAMINATION
PROVISIONAL GRADE SHEET

BRANCH : COMPUTER SCIENCE AND ENGINEERING

DATE:01.02.2014

SL NO.	U.S.N.	NAME OF THE STUDENTS	Engineering Mathematics - III		Computer Organization & Architecture		Data Structures		Logic Design		Microprocessors		HIGHER MATHEMATICS - I
			11MA3ICMAT (04 CREDITS)	GRADE POINTS	09CI3GCCOA (04CREDITS)	GRADE POINTS	09CI3GCDSL (06 CREDITS)	GRADE POINTS	09CI3GCLDL (05 CREDITS)	GRADE POINTS	09CI3GCMPL (06 CREDITS)	GRADE POINTS	11MA3IMDIP GRADE POINTS
167	1BM13CS414	ROOPASHREE S	B	8	X	0	S	10	A	9	A	9	PP
168	1BM13CS415	SAGAR V	F	0	B	8	B	8	X	0	B	8	PP

B.E III SEMESTER MARCH 2014 MAKE UP EXAMINATION
PROVISIONAL GRADE SHEET

BRANCH : COMPUTER SCIENCE AND ENGINEERING

DATE:19.05.2014

SL NO	U.S.N	NAME OF THE STUDENTS	Engineering Mathematics - III		Computer Organization & Architecture		Data Structures		Logic Design		Microprocessors		HIGHER MATHEMATICS - I
			11MA3ICMAT (04 CREDITS)	GRADE POINTS	09CI3GCCOA (04CREDITS)	GRADE POINTS	09CI3GCDSL (06 CREDITS)	GRADE POINTS	09CI3GCLDL (05 CREDITS)	GRADE POINTS	09CI3GCMPL (06 CREDITS)	GRADE POINTS	11MA3IMDIP GRADE POINTS
60	1BM13CS415	SAGAR V							B	8			

CONTROLLER OF EXAMINATIONS

PRINCIPAL

JFET

- The transverse electric field is developed across the reverse biased pn junction which controls the conductivity of the channel.
- The gate leakage current is about 10^{-19} A and input resistance is about $10^{8}\ \Omega$.
- The drain resistance of a JFET is about $1M\Omega$.
- JFET are complex to fabricate
- JFET are less susceptible to overload voltage.

MOSFET

- The Transverse electric field is induced across an insulating layer deposited on the semiconductor material which controls the conductivity of the channel.
- The gate leakage current is about 10^{14} A and input resistance is of the order of 10^{10} to $10^{15}\ \Omega$.
- The drain resistance of a MOSFET is about $50k\Omega$
- MOSFETs are easier to fabricate than JFET.
- MOSFET is very susceptible to overload voltage and needs special handling during installation.

Differences Between NMOS and PMOS.

PMOS

- Much easier and cheaper for to manufacture than N-channel MOSFET
- The holes mobility is 2.5 times less than electron mobility. Hence MOSFET requires larger area than an N-channel MOSFET having same current rating.
- PMOS are used in low and medium frequency switching applications
- The drain resistance is More than NMOS. (Three times more)

NMOS

- N-channel MOSFET is less popular Compared to P-channel MOSFET.
- For same current rate N-channel MOSFET requires less area
- As depletion region is thin, these are used in high frequency switching applications
- The drain resistance is less than PMOS.

In an N-channel JFET, $a = 3.75 \times 10^{-4}$ cm and $N_D =$ 10^{21} electrons/m^3, determine

(a) The pinch-off voltage

(b) The channel width at $V_{GS} = \frac{V_p}{2}$ and $I_D = 0$.

Assume $\mathcal{E} = 15\mathcal{E}_0$.

Given.

$a = 3.75 \times 10^{-4}$ cm $= 3.75 \times 10^{-6}$ m

$N_D = 10^{21}$ electrons/cm^3 $= 10^{21}$ electrons/m^3

$V_{GS} = \frac{V_p}{2}$

$I_D = 0$

$\mathcal{E} = 15\mathcal{E}_0 = 15 \times 8.854 \times 10^{-12} = 1.328 \times 10^{-10}$

(1) Pinch-off voltage

$$V_p = \frac{qN_D}{2\mathcal{E}} a^2 = \frac{1.6 \times 10^{-19} \times 10^{21} \times (3.75 \times 10^{-6})^2}{2 \times (1.328 \times 10^{-10})}$$

$$V_p = 8.471 \text{ V}$$

(2) $$b(x) = a\left[1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}\right] = 3.75 \times 10^{-4}\left\{1 - \left[\left(\frac{8.471}{2}\right)/8.471\right]^{1/2}\right\}$$

$$b(x) = 1.0983 \times 10^{-4} \text{ cm}$$

(2) Assume ... 4.9 V and the drain current changes from 1.2 mA to 1.75 mA. What is the value of transconductance?

$\Delta I_D = 1.75\ mA \sim 1.2\ mA = 0.55\ mA$

$\Delta V_{GS} = 5.10\ mA \sim 4.9\ V = 0.2\ V$

$$\text{Transconductance } g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.55\ mA}{0.2\ V} = \underline{\underline{2.75\ m\cdot\mho}}$$

(3) The drain current of a JFET is about 6 mA. When I_{DSS} is equal to 12 mA, $V_{GS(off)} = V_p = -6\ V$, determine the value of V_{GS}.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$\frac{V_{GS}}{V_{GS(off)}} = \left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$V_{GS} = V_{GS(off)}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$V_{GS} = (-6)\left[1 - \sqrt{\frac{6\times10^{-3}}{12\times10^{-3}}}\right]$$

$$\underline{\underline{V_{GS} = -1.757\ V}}$$

(4) In an N-channel FET has the following parameter $I_{DSS} = 15\ mA$, $V_p = -7\ V$ and $g_{mo} = 4500\ \mu S$. Determine the value of the drain current, and transconductance at $V_{GS} = -6\ V$.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 = \underline{\underline{306.12\ \mu A}}$$

$$g_m = \frac{-2i_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right] \text{ but } g_{mo} = \frac{-2i_{DSS}}{V_p}$$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_p}\right] = 642.857\ \mu\mho$$

Amplifiers.

Introduction.

→ Amplifier is an electronic circuit the increases the amplitude of applied input signal.

The input signal will be either voltage or current, and correspondingly the output signal will be voltage or current

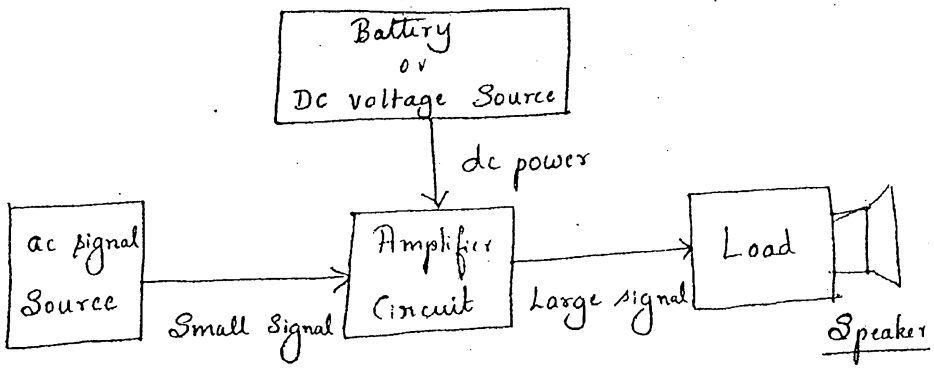


Figure 1: Block diagram of an audio amplifier system.

→ Figure 1 shows the block diagram of an audio amplifier. The dc voltage source is connected to the amplifier and it is used as source of energy for amplification.

→ Amplifiers consists of transistors that must be biased in the active region. so that the transistors can act in amplifiers

→ The microphone generates a very small signal in millivolt range and the amplifier produces a large output voltage

→ The output of the speaker should be exactly same as input signal of the microphone. i.e, output signal will be linearly proportional to the input signal.

→ The input signal is an analog signal. The amplitude of an analog signal will be of any value within limits and can vary continously with time. When an electronic circuit processes analog signal, it is called analog circuit.

→ Amplifier circuit is an analog circuit, it is used in radio, television, mobile phones and any communication equipments.

→ Active devices such as BJT and FET are commonly used in amplifier circuit.

Linear and Non-Linear Amplifiers

Linear Amplifier :- Electronic circuit whose output is directly proportional to its input signal, but it has capability to deliver more power into load.

Eg: Radio Frequency (RF) power amplifiers.

Non Linear Amplifiers :- It is one in which the output signal is not directly proportional to the input signal

Eg :- Nonlinear power amplifiers, integrator, differentiators.

In a Linear amplifier, the superposition theorem can be applied. The principle of superposition theorem states that the output of a linear circuit excited by multiple independent input signals is the sum of the outputs of the circuit corresponding to each of inout signals alone.

There are two types of analysis in linear amplifier circuits

① dc analysis

In dc analysis, the following steps are adopted.

ⓐ Initially, all ac sources are set to zero. Therefore, ac voltage source is replaced by short circuit and current source replaced by open circuit.

ⓑ All capacitors are replaced by open circuit

This analysis is known as large-signal analysis, which establishes the Q-point of the transistor.

② ac Analysis

It is performed by the following steps.

ⓐ All dc sources set to zero

ⓑ All coupling capacitors are short circuit

ⓒ Replace BJT with its small signal model

ⓓ Solve KCL and KVL equations to determine voltage and current

ⓔ Determine cut-off frequencies of the amplifier circuit.

The total response of the amplifier circuit is the sum of the responses of dc analysis and ac analysis.

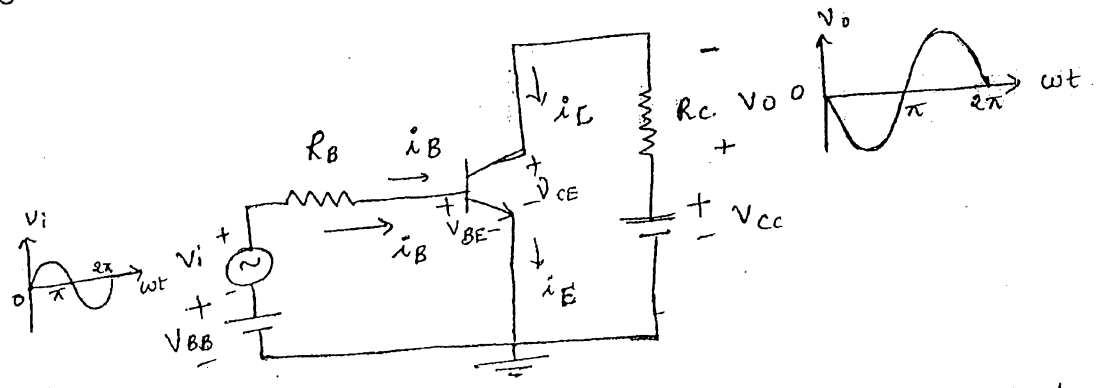
Classification of amplifiers

1. Based on Transistor Configuration
   - Common-Emitter (CE) amplifier.
   - Common-Collector (CC) amplifier.
   - Common-Base (CB) amplifier.
2. Based on input signal
   - Small Signal amplifier
   - Large Signal amplifier
3. Based on output
   - Voltage amplifier
   - Power amplifier
4. Based on active device
   - BJT amplifier
   - FET amplifier
5. Based on operating Condition
   - class A amplifier
   - class B amplifier
   - class C amplifier
   - Class D amplifier
   - Class AB amplifier
6. Based on frequency
   - Audio frequency (AF) amplifier
   - Intermediate frequency (IF) amplifier
   - Radio frequency (RF) amplifier.
7. Based on number of stages
   - Single Stage amplifier
   - Multistage amplifier
8. Based on method of Coupling between two stages.
   - Direct coupling amplifier
   - RC coupled amplifier
   - Transformer Coupled amplifier

BJT As a Linear Amplifier.

→ The below figure shows BJT which acts as linear amplifier, In this circuit, the base-emitter junction is forward biased and collector-base junction is reverse biased by V_{cc}. Then the transistor acts in active region.

V_i is sinusoidal ac input voltage. The ac input signal V_i is such that it always forward biases the emitter base junction regardless of polarity of ac input voltage signal V_i.

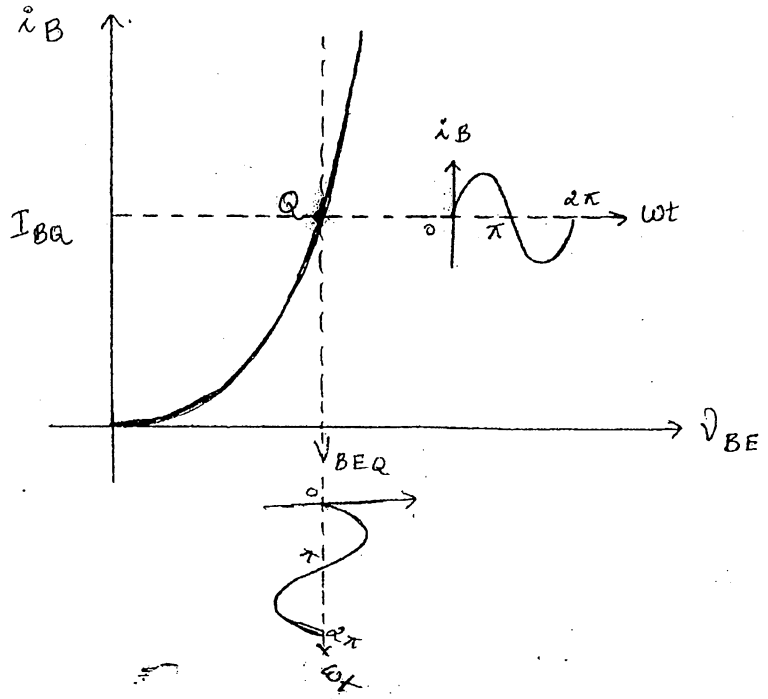


→ Initially assume that there is no ac signal. Then dc base current I_B flows through R_B and the collector current flows through R_c. This current is known as quiescent operating current

→ When an ac signal is applied between the emitter-base junctions, the forward bias between emitter-base junction is increased during positive half cycle of input ac signal Consequently more electrons are injected into the base and they reach the collector. Due to increase in collector current I_c the voltage drop across R_c is increased.

→ In the negative half cycle of input ac voltage v_i, the forward bias voltage across the emitter base junction decreases. Subsequently, the collector current decreases and voltage drop across R_c decreases.

→ The time varying input voltage v_i across the Base-emitter junction generates a time varying base current i_B as shown below.



The notations used for different current and voltages of BJT are.

I_B → dc base current
V_{BE} → dc base to emitter voltage
I_C → dc collector current
V_{CE} → dc collector to emitter voltage
i_b → ac base current
v_{be} → ac base to emitter voltage
i_c → ac collector current
v_{ce} → ac collector to emitter voltage.

I_{BQ} → Q-point base current
V_{BEQ} → Q-point base to emitter voltage
I_{CQ} → Q-point collector current
V_{CEQ} → Q-point collector to emitter voltage
i_B → Instantaneous base current
v_{BE} → Instantaneous base to emitter voltage
i_C → Instantaneous collector current
v_{CE} → Instantaneous collector to emitter voltage

i_B is the total instantaneous value of base current $i_B = i_b + I_B$

v_B is the total instantaneous value of base emitter voltage

$$v_{BE} = V_{BE} + v_{be}$$

Using diode current equation relationship between the ac base emitter voltage and ac base current is

$$i_B = \frac{I_S}{\beta} e^{\frac{v_{BE}}{V_T}}$$

$$v_{BE} = V_{BEQ} + v_{be}$$

$$\therefore \quad i_B = \frac{I_S}{\beta} e^{\frac{V_{BEQ}}{V_T}} \cdot e^{\frac{v_{be}}{V_T}}$$

Since $\frac{I_S}{\beta} e^{\frac{V_{BEQ}}{V_T}}$ is called Q-point base current

$$i_B = I_{BQ} e^{\frac{v_{be}}{V_T}}$$

The base current i_B is nonlinear and cannot be represented by superposition of an ac current and dc quiescent current.

Using taylor series expansion

$$e^x = 1 + \frac{x}{1!} + \frac{1}{2!}x^2 + \frac{1}{3!}x^3 + \cdots$$

The equation for i_B can be expanded as.

$$i_B = I_{BQ}\left[1 + \frac{v_{be}}{V_T} + \frac{1}{2}\left(\frac{v_{be}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_{be}}{V_T}\right)^3 + \cdots\right]$$

$$i_B = I_{BQ}\left[1 + \frac{v_{be}}{V_T}\right]$$ as $V_T \gg v_{be}$ and $\left[\frac{v_{be}}{V_T}\right]^2$ can be neglected.

$$i_B = I_{BQ} + I_{BQ}\frac{v_{be}}{V_T}$$

$$i_B = I_{BQ} + i_b$$ where $i_b = \frac{I_{BQ}}{V_T} v_{be}$ is sinusoidal base current.

→ When a time varying ac signal is super imposed on dc voltage V_{BB}, the output voltage can be generated which is also time varying and it has 180° phase shift. Since the amplitude is time varying output voltage v_o is directly proportional to the ac input voltage v_i, this circuit is called linear amplifier.

Applying superposition theorem to linear circuit, we obtain.

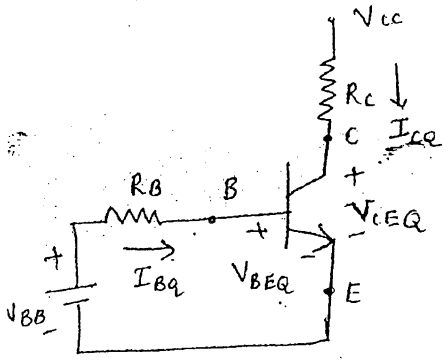
$$i_B = I_{BQ} + i_b$$

$$i_C = I_{CQ} + i_c$$

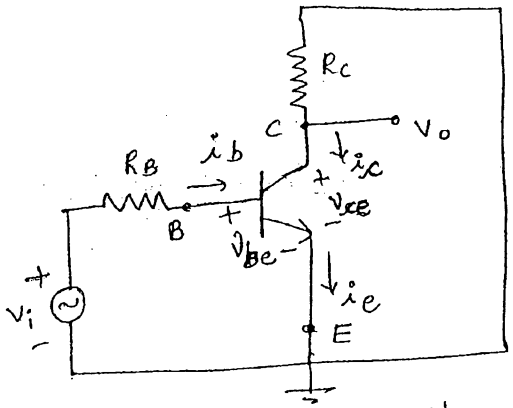
$$v_{BE} = V_{BEQ} + v_{be}$$

$$v_{CE} = V_{CEQ} + v_{ce}$$

The dc and ac equivalent circuits of CE amplifier are.



dc equivalent circuit



—— ac equivalent circuit.

In dc equivalent circuit KVL equation in base emitter loop

$$V_{BB} = I_{BQ} R_B + V_{BEQ}.$$

Collector - emitter loop.

$$V_{CC} = I_{CQ} R_C + V_{CEQ}.$$

When ac signal is incorporated in base emitter loop equation

$$V_{BB} + v_i = i_B R_B + v_{BE}$$

$$= (I_{BQ} + i_b) R_B + (V_{BEQ} + v_{be})$$

$$= I_{BQ} R_B + i_b R_B + V_{BEQ} + v_{be}$$

$$V_{BB} + v_i = I_{BQ} R_B + V_{BEQ} + i_b R_B + v_{be}$$

But $V_{BB} = I_{BQ} R_B + V_{BEQ}$ hence.

$$v_i = i_b R_B + v_{be}$$

This base-emitter loop equation is justified only when an ac signal is present.

The collector emitter loop equation can be written as.

$$V_{CC} = i_C R_C + v_{CE}$$

$$= (I_{CQ} + i_c) R_C + (V_{CEQ} + v_{ce})$$

$$V_{CC} = I_{CQ} R_C + V_{CEQ} + i_c R_C + v_{ce}$$

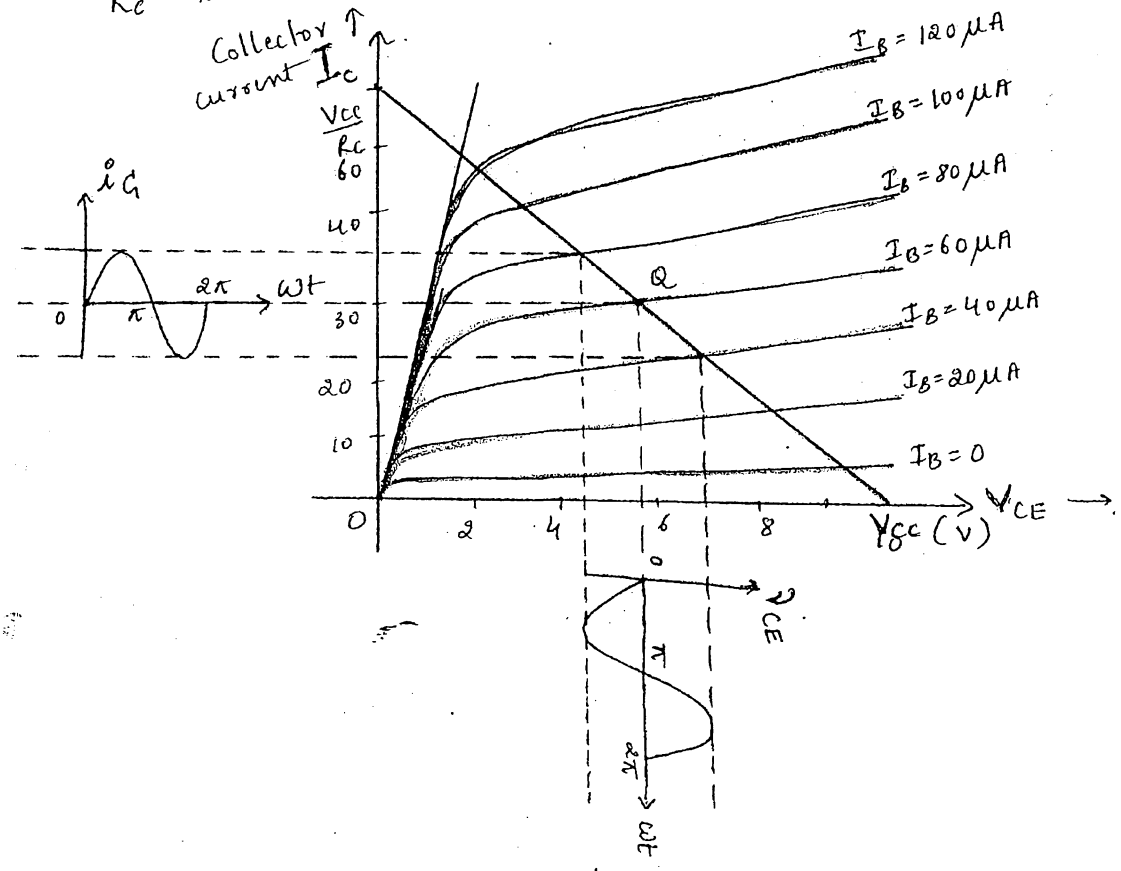
But $V_{CC} = I_{CQ} R_C + V_{CEQ}$ hence.

$$i_c R_C + v_{ce} = 0.$$

This is the collector-emitter loop equation only when an ac signal is present and all the dc terms are set to zero.

The below figure shows the output characteristics of CE amplifier with dc load Line.

Due to sinusoidal input voltage v_i, a time varying base current flows through base of BJT. Then time varying base current generates an ac collector current which is superimposed on the Q-point collector current. Subsequently, voltage across R_c is ac and collector emitter voltage is also ac.

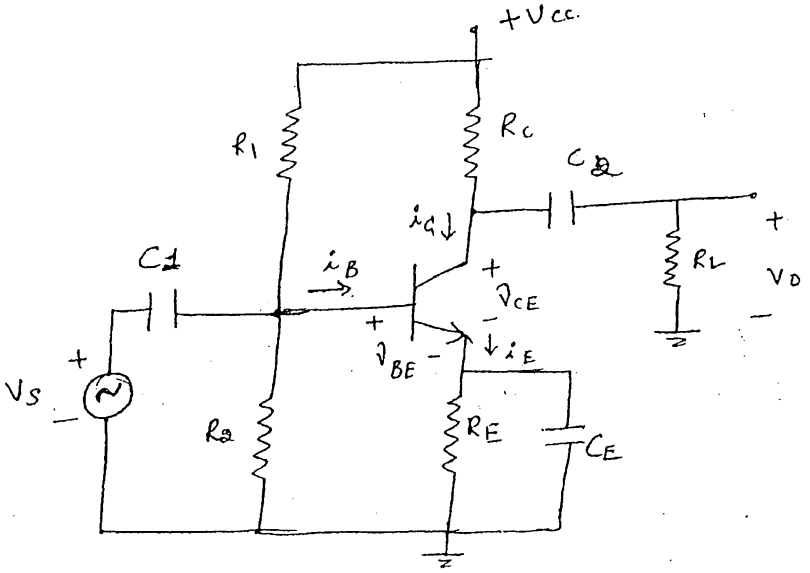


Characteristics of CE amplifier.

1. It has large voltage gain A_v. The value of A_v is about 1500
2. Its current gain is high. The value of A_I is about 50 to 300
3. It has very high power gain (A_p). Its value is about 10,000
4. Input impedance is moderately low its value is in the range of 1kΩ to 2kΩ
5. The input impedance is moderately large its value is about 50k

CE Amplifier (Common Emitter) with Voltage divider Bias.

The common emitter circuit with voltage divider bias is shown in below figure.



→ The resistors R_1 and R_2 act as potential dividers at base terminal of transistor.
R_E provides the stabilization against the variation of bias point due to change in β value.

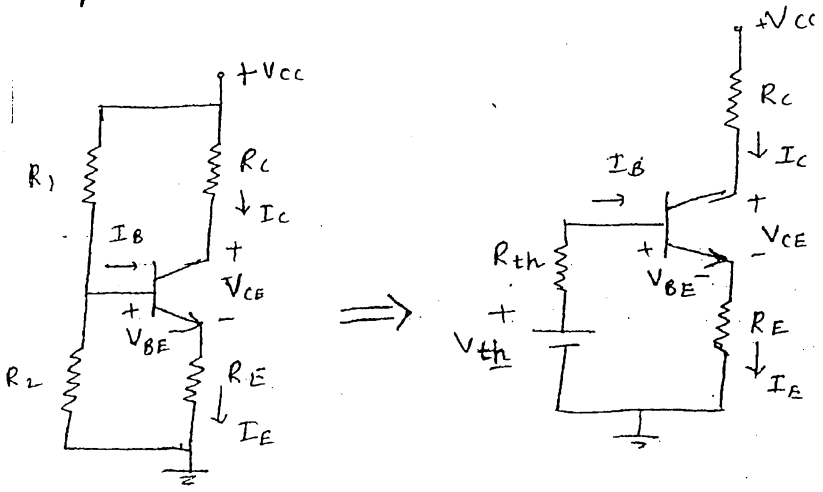
→ C_1 and C_2 are coupling capacitors. These capacitors are also known as blocking capacitors. as they block dc signal from input and output terminals.

→ C_E is the emitter capacitor. This capacitor is also known as bypass capacitor as due to presence of C_E the emitter terminal is connected to ground for ac current. The bypass capacitor acts as an open circuit for dc current.

dc Analysis.

The dc equivalent circuit can be obtained by short circuiting ac voltage source and open circuiting capacitors.

The dc equivalent circuit is as shown in below figure.



dc equivalent circuit

Thevenin's equivalent circuit

→ The dc equivalent circuit can be replaced by thevenine equivalent circuit where

$$V_{th} = V_{CC}\frac{R_2}{R_1+R_2} \quad \text{and} \quad R_{th} = R_1 \| R_2.$$

Applying KVL to base emitter loop.

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E$$

Ap. $I_E = I_B + I_C$ and $I_C = \beta I_B$ V_{th} can be written as

$$V_{th} = I_B R_{th} + V_{BE} + (\beta I_B + I_B) R_E$$

$$V_{th} = I_B\left[(\beta+1)R_E + R_{th}\right] + V_{BE}$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta+1)R_E}$$

$$I_C = \beta I_B \quad \text{and} \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

ac Analysis (Using re model)

→ For small signal analysis of BJT, it is required to develop a small signal equivalent circuit.

→ In re model, the resistance values and β are required for proper circuit analysis

The advantages of re model of BJT are

(a) Required parameters are available very easily
(b) Analysis is very simple and easy.
(c) Accuracy of circuit analysis is good.

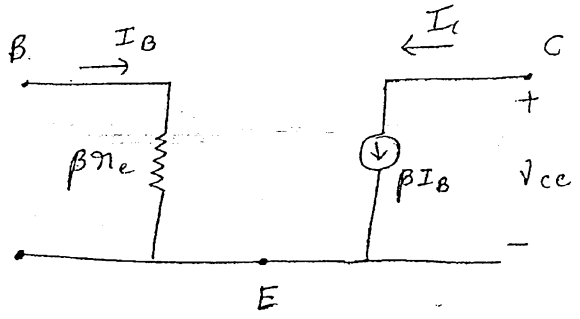
→ In a common emitter configuration, the collector current I_C is β times base current I_B. The ac resistance of the base emitter junction is equal to

$$r_{ac} = \frac{25\,mV}{I_B}$$

As $I_B = \frac{I_C}{\beta} \approx \frac{I_E}{\beta}$

$$r_{ac} = \frac{25\,mV}{\frac{I_E}{\beta}} = \beta \frac{25\,mV}{I_E} = \beta r_e$$

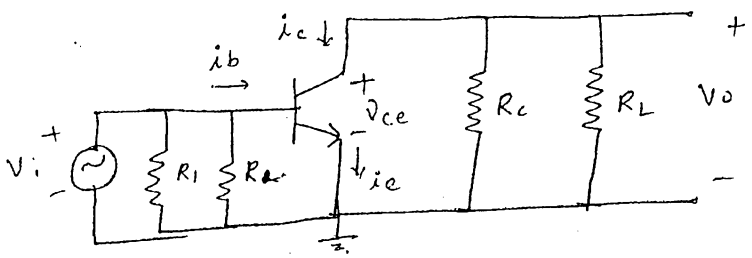
The re model of npn transistor in CE configuration can be written as.



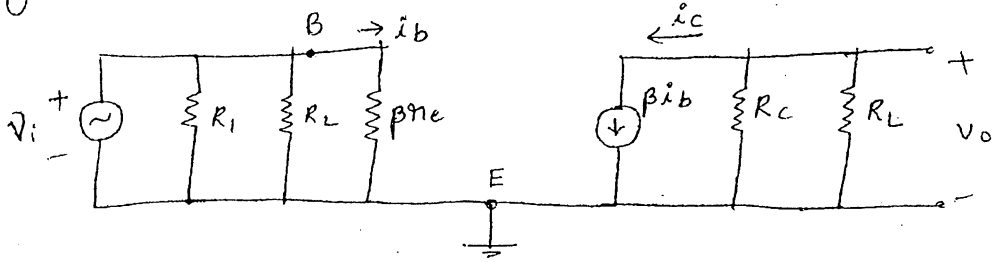
ac analysis of voltage divider bias circuit using r_e model.

→ The ac equivalent circuit can be obtained by short circuiting the dc voltage source and the capacitors.

The ac equivalent model of CE amplifier is as below



After replacing BJT with its r_e model we can get the circuit as shown below.



→ The input resistance $R_i = R_1 \,||\, R_2 \,||\, \beta r_e = R_{th} \,||\, \beta r_e$

→ The output resistance is determined when input is zero ($V_i = 0$)

The output resistance $R_o = R_c \,||\, R_L$

The ac Load of the circuit $r_L = R_c \,||\, R_L$

The input voltage is $V_i = \beta r_e i_b$ and output voltage $= -i_c r_L$

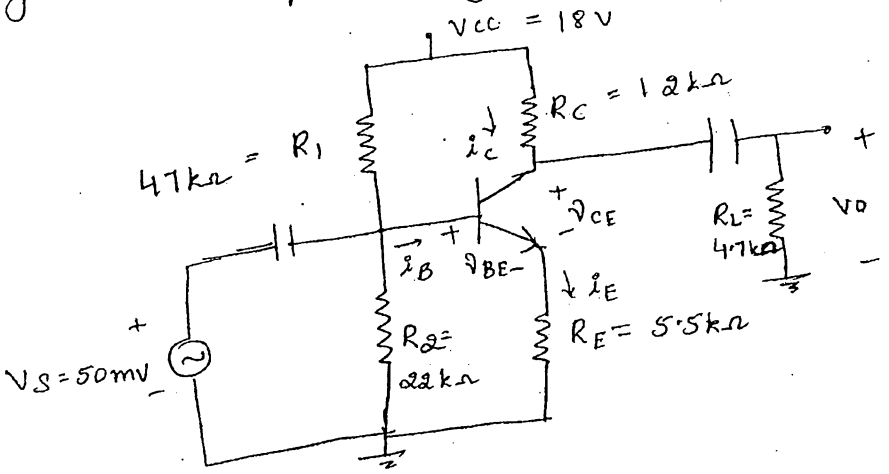
The voltage gain $A_V = \dfrac{V_o}{V_i} = \dfrac{-i_c r_L}{\beta r_e i_b} = \dfrac{-r_L}{r_e}$

The negative sign indicates that output voltage is 180° phase shifted from input voltage.

The current gain $= \dfrac{i_L}{i} = \dfrac{-i_o}{i_i} = \dfrac{-\beta i_b}{i_i}$

Problem

The below figure shows a common-emitter amplifier. Draw the ac equivalent circuit. Determine the input resistance, voltage gain and output voltage. Assume $\beta = 50$



Soln.

Given

$V_{cc} = 18\ V$

$R_c = 12k\Omega$

$R_E = 5.5k\Omega$

$R_1 = 47k\Omega$

$R_2 = 22k\Omega$

$V_s = 50mV$

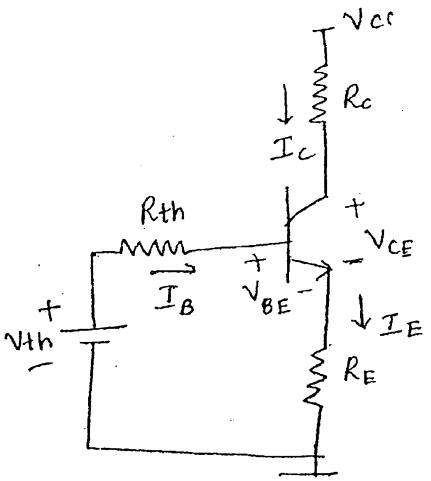
$\beta = 50$

The thevenine voltage $V_{th} = \dfrac{V_{cc} R_2}{R_1 + R_2}$

$$V_{th} = \frac{18 \times 22k}{47k + 22k} = \underline{\underline{5.739\ V}}$$

$$R_{th} = R_1 || R_2 = \underline{\underline{14.985\ k\Omega}}$$

The dc thevenine equivalent circuit is



Applying KVL to base emitter loop.

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E$$

$$V_{th} = \frac{I_C}{\beta} R_{th} + V_{BE} + I_E R_E$$

Assuming $I_C \cong I_E$

$$V_{th} = I_E \left(\frac{R_{th}}{\beta} + R_E \right) + V_{BE}$$

$$I_E = \frac{V_{th} - V_{BE}}{R_E + \frac{R_{th}}{\beta}} = \frac{5.739 - 0.7}{5.5 \times 10^3 + \frac{14.985 \times 10^3}{50}} = 0.8688 \text{ m}$$

The ac resistance of emitter $\longrightarrow$ $r_e = \frac{25 \text{mV}}{I_E} = 28.77$

(a) The input resistance looking from base

$$R_i = \beta r_e = 50 \times 28.77 \, \Omega = 1.4385 \text{ k}\Omega$$

The total input resistance.

$$R_{i\_total} = R_i || R_{th} = R_1 || R_2 || \beta r_e = 1.438 \text{ k} || 14.985 \text{k}$$

$$R_{i\_total} = 1.312 \text{ k}\Omega.$$

The ac load $r_L = R_c || R_L = 3.377 \text{ k}\Omega$

(b) Voltage gain $A_V = \frac{V_o}{V_i} = -\frac{r_L}{r_e} = 117.4$

(c) the output voltage,

The overall voltage gain $A_V = \frac{V_o}{V_s}$

$$117.4 = \frac{V_o}{50 \text{ mV}}$$

$$V_o = 5.87 \text{ V}$$

Comparison of CE, CB and CC amplifiers.

Parameters	CE (amplifier)	CB amplifier.	CC amplifier
Input resistance.	Moderate (βr_e)	low r_e	high βR_E
Output resistance	High R_c	High R_c	Low r_e
Input resistance	Low	Very low	High.
Current gain.	High β	Low, about 1	High $(1+\beta)$
Power gain	High.	Moderate	Low.
Phase shift	180°	0°	0°

A. OSCILLATORS

Introduction

In process of feedback a part of output is sampled and fed back to the input of the amplifier. This process improves the performance of amplifier and makes it more ideal.

When the input signal and part of the output which is fed back to the input are in phase with each other the feedback is called positive feedback.

The positive feedback generates oscillation and hence used in electronic circuits to generate oscillations of desired frequency. Such circuits are called oscillators.

Classification of Oscillators

Oscillators
- Based on output waveform.
  - (1) Sinusoidal or harmonic oscillators
    Eg: sine, cosine waves etc.
  - (2) Non-sinusoidal or relaxation
    Eg: Square, triangular, pulse etc.
- Based on circuit Components
  - (1) R and C
    Eg: RC phase shift oscillator
    wein bridge oscillator
  - (2) L and C
    Eg: Hartley and Colpit oscillators
- Based on range of operating frequency
  - (1) Audio Frequency (AF) oscillators
    20 Hz to 20k Hz
  - (2) Radio Frequency (RF) oscillators
    20 KHz to 30 MHz
  - (3) Very High frequency (VHF) oscillators
    30 - 300 MHz
  - (4) Ultra-High frequency (UHF) oscillators
    300 MHz to 3 GHz
  - (5) Microwave oscillators 3-300

Sinusoidal oscillations can be produced using two different types of principles.

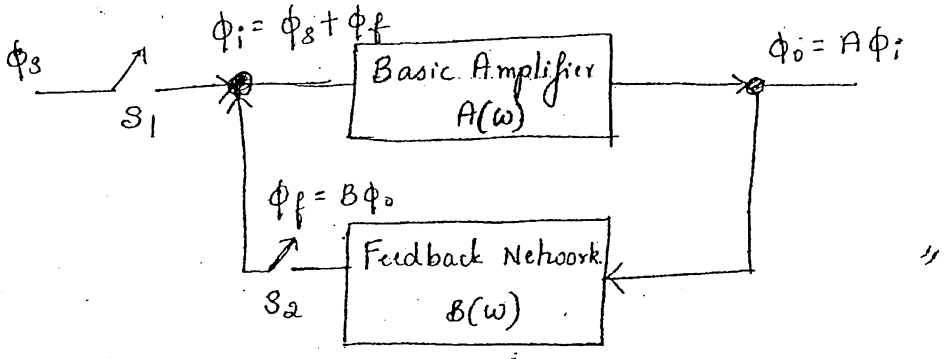
① Negative Resistance oscillators :- These are non feed back oscillators. The non-feedback oscillators use the negative resistance region of the characteristics of active device used. In negative resistance region as the voltage applied to device increases, the current flowing through the device decreases.
Eg: Tunned diode, UJT relaxation oscillator, Gunn oscillator.

② Feedback oscillators : Oscillators in which the feedback is used, which satisfies the required conditions.

Principle of Sinusoidal oscillation

→ The block diagram of basic structure of sinusoidal oscillation consists of a basic amplifier with gain $A(\omega)$ and feedback network with feedback factor $B(\omega)$. where $A(\omega)$ and $B(\omega)$ are frequency ($\omega = 2\pi f$) selective quantities.

→ The quantity ϕ represents either current or voltage signal.



Initially S_1 is closed and S_2 is opened i.e,

$$\phi_i = \phi_s \quad \text{and} \quad \phi_f = B(\omega)\phi_0 = B(\omega)A(\omega)\phi_i$$

The ratio $\frac{\phi_f}{\phi_i} = B(\omega)A(\omega) \longrightarrow$ Open loop gain.

$B(\omega)$ and $A(\omega)$ are functions of frequency. If for particular frequency $\omega = \omega_0$, we have $[B(\omega_0)A(\omega_0)] = 1$ and we get

$$\phi_f = \phi_i = \phi_s$$

Now if Switch S_1 is opened and S_2 is closed.

Hence at $\omega = \omega_0$ the feedback signal will have same magnitude as input signal and also in phase with input signal.

Hence the system will sustain oscillations at particular frequency $\omega_0 (2\pi f_0)$ even if $\phi_s = 0$

$$A_f = \frac{A(\omega)}{1 - A(\omega)B(\omega)}$$

if $[A(\omega_0)B(\omega_0)] = 1$ then $A_f = \infty$

This indicates that the circuit can produce output without external input ($V_s = 0$), just by feeding the part of the output as its own input.

Similarly, output cannot be infinite but gets driven into the oscillations. In other words, the circuit stop amplifying and starts oscillating.

Barkhausen Criteria

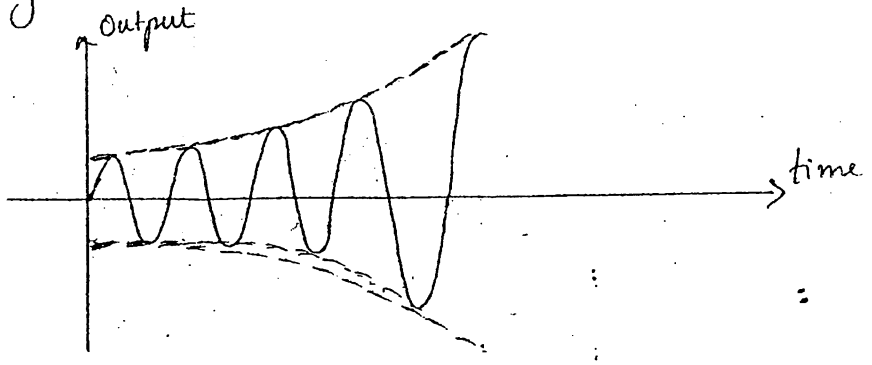
Since $A(\omega)$ and $B(\omega)$ are complex quantities, they give two conditions.

① $|A(\omega) \cdot B(\omega)| = 1 \Rightarrow$ The magnitude of the product of the open loop gain of the amplifier $[A(\omega)]$ and the magnitude of the feedback factor β is unity.

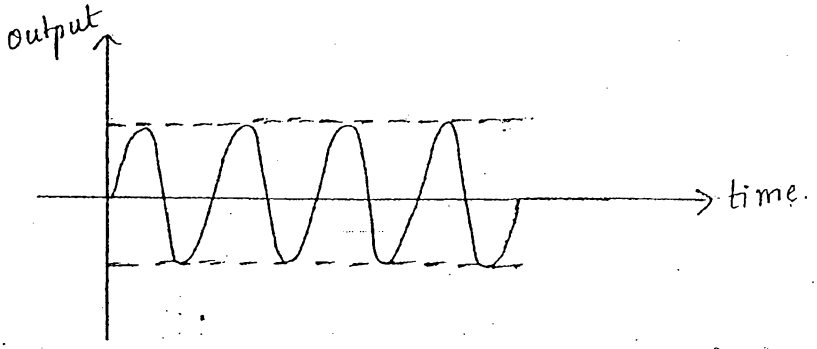
② $\underline{|A(\omega) \cdot B(\omega)} = 1 \Rightarrow$ The total phase shift around a loop, as the signal proceeds from input through amplifier, feedback network back to input again, completing a loop, is precisely 0° or 360°.

In practice, $[A(\omega)B(\omega)]$ is made greater than 1 to start the oscillations and then the circuit adjusts itself to get $[A(\omega)B(\omega)] = 1$, finally resulting into self sustained oscillations. Below cases give the effect of the magnitude of the product $|A(\omega)B(\omega)|$ on nature of oscillations.

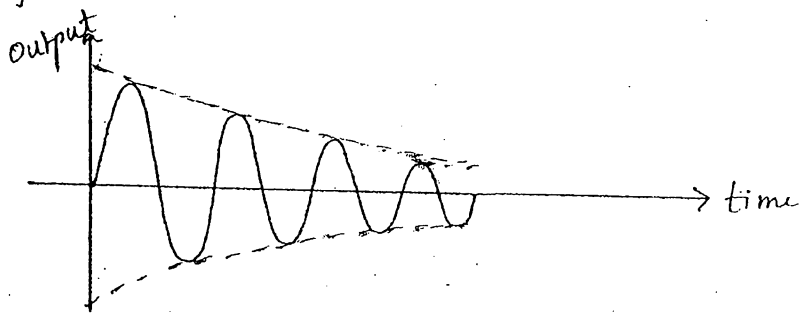
Case 1: If phase shift around loop is 0° or 360° and $|A(\omega)B(\omega)| > 1$, then output oscillates but oscillations goes on increasing as shown in the figure below



Case 2: If phase shift around the loop is 0° or 360° and $|A(\omega)B(\omega)| = 1$ Then oscillations are with constant amplitude and frequency. (sustained oscillations)



Case 3: when total phase shift around loop is 0° or 360° but $|A(\omega)B(\omega)| < 1$ then the oscillations are of decaying type.

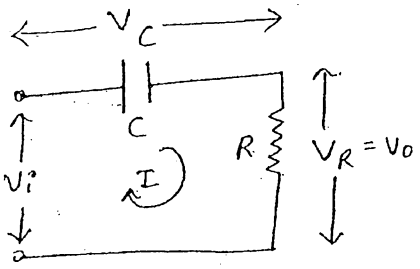


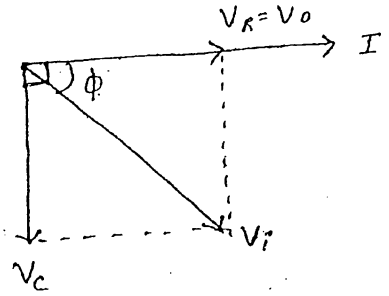
Case 4: If magnitude $|A(\omega)B(\omega)| = 1$ but $|A(\omega)B(\omega)| \neq 0$ then oscillation will die out, because input signal will gradually decay due to phase cancellation of signal fed back to the input after successive trips around the loop.

RC Phase Shift Oscillator

→ RC phase shift oscillator basically consists of an amplifier and a feedback network, consisting of resistors and capacitors. arranged in ladder fashion.

→ Let consider a RC circuit, which is used in the feedback network of oscillator.





→ Let current I flows through R and C.

→ V_o is the voltage drop across R and V_c is the voltage across capacitor C.

→ V_o is in phase with current I, where V_c lags behind I by 90°.

The vector sum of V_o and V_c is V_i. There is a phase difference of ϕ between input and output voltage (V_o & V_i)

From Ckt $V_o = IR$.

$V_c = IX_c$.

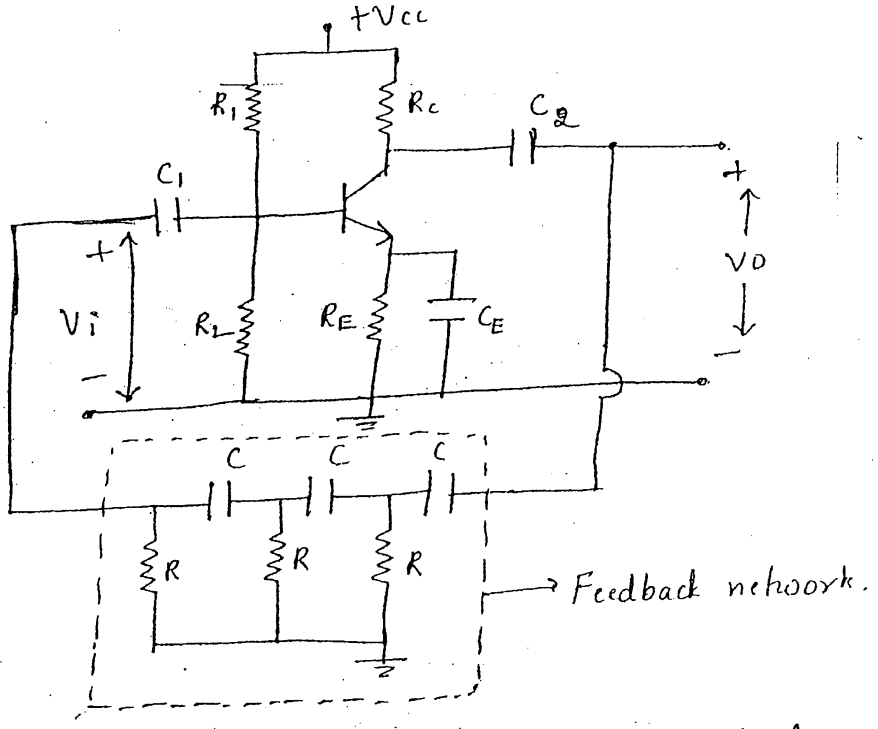
From phasor diagram

$$\tan\phi = \frac{V_c}{V_R} = \frac{IX_c}{IR} = \frac{1}{2\pi fCR}$$

$$\boxed{f = \frac{1}{2\pi CR \tan\phi}}$$

→ In RC phase shift oscillator three RC sections are used. By using proper values of R and C, the angle ϕ is adjusted to 60°. Total phase shift will be 180°

In RC phase shift oscillator CE, single stage amplifier is used as a basic amplifier. This produces 180° phase shift. The feedback network consists of 3 RC sections each producing 60° phase shift. This circuit is shown below.



The total phase shift around the loop is 180° of amplifier and 180° due to 3 RC stages, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.

The frequency of sustained oscillations generated depends on the values of R and C.

$$f = \frac{1}{2\pi\sqrt{6}\,RC} \quad (Hz)$$

LC Tuned Circuit Operation (LC Tank Circuit)

The LC tank circuit consists of elements L and C connected in parallel as shown below.

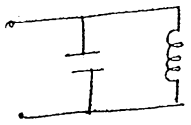


figure (a)

Let capacitor is initially charged from a dc source with the polarities as shown in below figure.

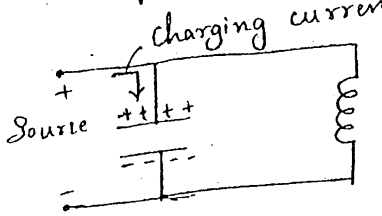


Figure (b)

When the capacitor gets fully charged energy stored in capacitor is electrostatic energy. Then the capacitor starts discharging through L in the direction of flow of conventional current I. in fig c. Due to such current the magnetic field gets set up around the inductor L. Thus inductor starts storing the energy when the capacitor is fully discharged, maximum current flows through the circuit and all the electrostatic energy get stored as a magnetic energy in the inductor L as shown in figure d.

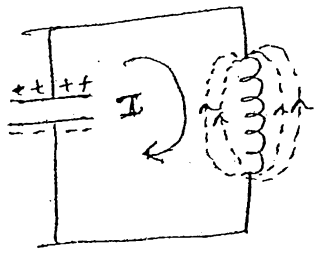


Figure (c)

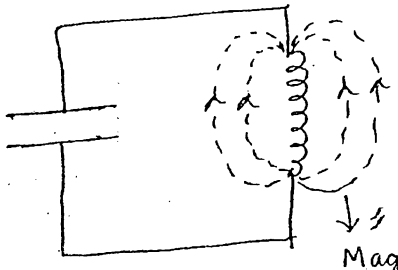


Figure (d)

Now the magnetic field around L starts collasping. As per Lenz's law, this starts charging the capacitor with oppopite polarity making lower plate positive and upper plate negative as shown in figure (e)

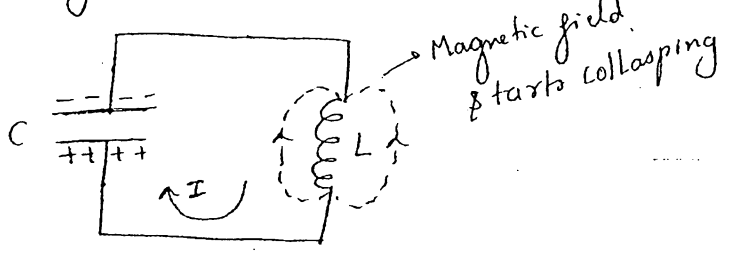


Figure (e)

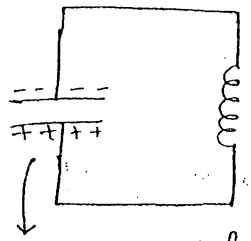


Figure (f)

After some time, capacitor gets fully charged with oppopite polarity as compared to ith initial polarity. as shown in figure (f).

Now the capacitor again starts to discharge through inductor L, But in oppopite direction as shown in figure (g)

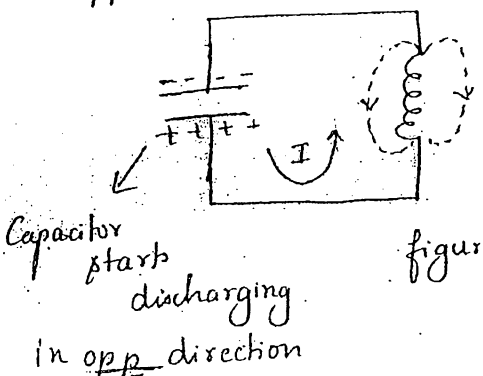


figure: (g)

This is nothing but oscillatory current. But every time when energy is transfered from C to L and L to C the losses occure due to which the amplitude of oscillating current keeps on decreasing. Hence we get exponentially decaying signals called damped oscillations.

The feedback n/w consists of two inductors L_1 and L_2 and capacitor C.

The transistor amplifier provides a phase shift of 180°. When power supply V_{cc} is ON, Collector current starts rising and charges the capacitor when the capacitor is fully charged it discharges through coil L_1 and L_2. Thus damped oscillations are set up in the tank circuit. The oscillations across L_1 are applied to the input circuit and appeared in amplified form in the output circuit.

Continous undamped output is obtained as a result of continous supply of energy to the tank circuit to overcome the losses occuring in it.

The frequency of oscillation is produced by LC tank circuit

$$f = \frac{1}{2\pi\sqrt{LC}}$$

There are two inductors L_1 and L_2. There exists a mutual inductance M between two inductors the total inductance is

$$L_{eq} = L_1 + L_2 + 2M$$

Hence frequency of oscillation becomes

$$\boxed{f = \frac{1}{2\pi\sqrt{L_{eq}C}}}$$

To satisfy Barkhausen criteria The open loop gain.

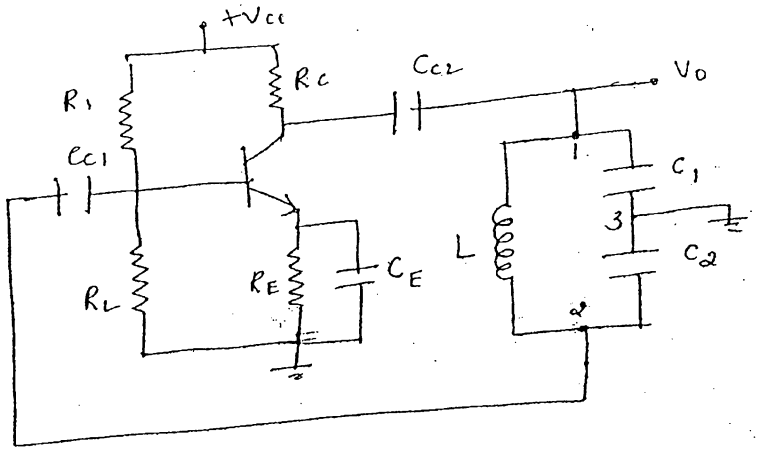
$$A = \frac{X_1}{X_2} = \frac{2\pi f L_1 + 2\pi f M}{2\pi f L_2 + 2\pi f M} = \frac{L_1 + M}{L_2 + M}$$

$$\boxed{A = \frac{L_1 + M}{L_2 + M}}$$

Colpitts Oscillator

The tank circuit of Colpitts oscillator uses two capacitors and one inductor. The two capacitors are C_1 and C_2 which are connected in series across inductor L.

The circuit below shows Transistorised Colpitts oscillator.



When the power supply switch is ON, capacitors C_1 and C_2 are charged and then discharged through the inductor L, thereby generating damped harmonic oscillations in the tank circuit. The CE amplifier produces a phase change of 180°. between input and output and tank circuit provides additional phase change of 180° so total change at the input of amplifier is 360°. and positive feedback is established. Hence continous undamped oscillations are produced.

The frequency of oscillations in colpitts oscillator is

$$f = \frac{1}{2\pi\sqrt{LC}}$$

There are two capacitors ~~with~~ C_1 and C_2 in series hence

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

$$\therefore f = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

Condition of maintenance of oscillations, the open loop gain

$$A = \frac{X_1}{X_2} = \frac{\frac{1}{2\pi f C_1}}{\frac{1}{2\pi f C_2}} = \frac{C_2}{C_1}$$

$$\boxed{A = \frac{C_2}{C_1}}$$

Crystal Oscillator

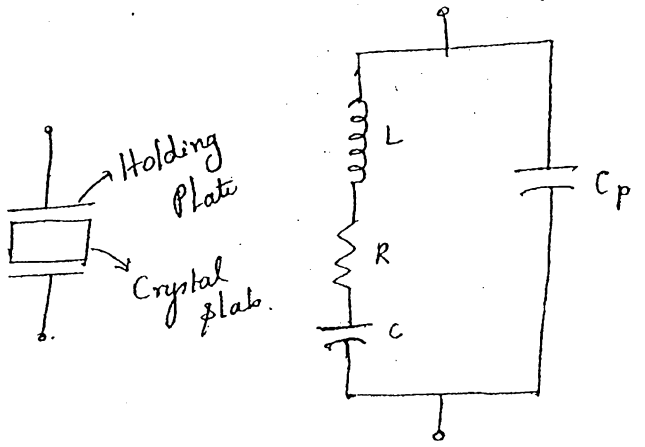
→ Frequency of oscillation of Hartley and Colpitts oscillator depends on the values of tank circuit parameters. These parameters change with time, temperature etc. For higher stability crystal oscillators are used.

→ The crystals are naturally occuring or synthetically manufactured circuit component. The oscillations are produced by the crystals due to Piezoelectric Effect.

→ The piezoelectric effect means under the influence of mechanical pressure, ac voltage gets generated across the opposite faces of the crystal. Conversely if the crystal is subjected ac voltage it vibrates causing mechanical distortion in its shape. Every crystal has its own resonating frequency associated with it depending on its cut.

When frequency of applied ac voltage is equal to natural frequency of the crystal, the amplitude of mechanical oscillations become maximum.

AC equivalent circuit of vibrating crystal is represented by a series of LCR circuit shunted by capacitor C_p as shown below.



→ The shunt capacitance C_p represents the electrostatic capacitance between two metal plates separated by a dielectric like crystal slab. It is called Mounting capacitance.

→ When crystal is vibrating, there will be internal frictional losses denoted by a resistance R. The inductor L indicates the crystal mass. (indication of its inertia). In vibrating the crystal will have mechanical stiffness indicated by C.

The expression for resonating frequency is in range of few KHz to 100 MHz, Eg: Rochelle salt, Quartz crystal, tourmaline

The crystal has 2 frequencies associated with.

a series resonance frequency

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

a parallel resonance frequency

$$f_r = \frac{1}{2\pi\sqrt{L C_{eq}}}, \quad \text{where } C_{eq} = \frac{C C_p}{C + C_p}.$$

Problems

1) In a RC phase shift oscillator, the phase shift n/w uses resistances each of 4.7 kΩ and capacitors each of 0.47 μF find frequency of oscillation.

Given

$R = 4.7\ k\Omega$

$C = 0.47\ \mu F$

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

$$f = \frac{1}{(2\pi)(\sqrt{6})(4.7\times10^{3})(0.47\times10^{-6})}$$

$$f = 29.413\ Hz.$$

2) Design RC phase shift oscillator using CE amplifier. for frequency 900 KHz.

$f = 900\ KHz$

Let $C = 1\ pF$

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

$$R = \frac{1}{(2\pi)\sqrt{6}(900\times10^{3})(1\times10^{-12})}$$

$$R = 72.1941\ k\Omega$$

3) In a Colpitts oscillator the desired frequency is 500 KHz estimate L, assuming $C = 1000\ pF$

For Colpitts oscillator $C_1 = C_2 = C = 1000\ pF$

$$C_{eq} = \frac{C_1C_2}{C_1+C_2} = 500\ pF$$

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} \Rightarrow L = \frac{1}{(2\pi f)^2 C_{eq}}$$

$$L = 202.64\ \mu H$$

(4) Design the value of an inductor to be used in Colpitts oscillator to generate a frequency of 10 MHz. The circuit is used capacitor $C_1 = 100\,pF$ and $C_2 = 50\,pF$

Given

$C_1 = 100\,pF$

$C_2 = 50\,pF$

$f = 10\,MHz$.

$L = ?$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = 33.33\,pF$$

$$f = \frac{1}{2\pi\sqrt{L C_{eq}}} \Rightarrow L = \frac{1}{(2\pi f)^2 C_{eq}}.$$

$$f = 7.6\,\mu H$$

(5) Calculate frequency of oscillations of Hartley oscillator having $L_1 = 0.5\,mH$, $L_2 = 1\,mH$ and $C = 0.2\,\mu F$.

Given

$L_1 = 0.5\,mH$

$L_2 = 1\,mH$

$C = 0.2\,\mu F$

$$f = \frac{1}{2\pi\sqrt{L_{eq} C}}$$

$$L_{eq} = L_1 + L_2 = 1.5\,mH$$

$$f = 9.18\,kHz.$$

(6) In a Hartley oscillator $L_1 = 20\,\mu H$, $L_2 = 2\,mH$ and C is variable Find range of C if frequency is to be varied from 1MHz to 2.5 MHz. Neglect mutual inductance.

given

$L_1 = 20\,\mu H$

$L_2 = 2\,mH$

$f_1 = 1\,MHz$

$f_2 = 2.5\,MHz$

$L_{eq} = L_1 + L_2 = 2.02\,mH$

$f_1 = 1\,MHz$. $f = \frac{1}{2\pi\sqrt{L_{eq} C}}$

$$C_1 = \frac{1}{(2\pi f_1)^2 L_{eq}} = 12.539\,pF$$

$f_2 = 2.5\,MHz$

$$C_2 = \frac{1}{(2\pi f_2)^2 L_{eq}} = 2.006\,pF$$

(11) In a crystal $L = 0.4\ H$, $C = 0.085\ pF$ and $C_p = 1\ pF$ with $R = 5\ k\Omega$. Find

(1) Series resonant frequency

(2) Parallel resonant frequency

(3) By what percent does the parallel resonant frequency exceed the series resonant frequency

(1) $$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.4 \times 0.085 \times 10^{-12}}} = 863.138\ kHz$$

(2) $$C_{eq} = \frac{CC_p}{C + C_p} = 7.883 \times 10^{-14}\ F$$

$$f_p = \frac{1}{2\pi\sqrt{L C_{eq}}} = \frac{1}{2\pi\sqrt{0.4 \times 7.883 \times 10^{-14}}}$$

$$f_p = 900\ kHz$$

(3) Percentage increase $= \frac{900\ kHz - 863.138\ kHz}{863.138\ kHz} \times 100 = 4.27\%$

Introduction to Frequency Response of BJT amplifiers

→ The gain of amplifier is function of frequency.

→ The frequency response is a plot of amplifier gain (dB) versus frequency (Hz) [That is on logarithmic scale]

General Frequency Response of Amplifiers.

→ The frequency of the applied input signal has a significant effect on the frequency response of the single-stage and multistage amplifiers.

→ At low frequencies, the effect of coupling and bypass capacitors cannot be neglected due to capacitive reactance value.

At high frequencies, the frequency dependent parameters will be present in the circuit and stray capacitance will be present with small-signal model of BJT.

The frequency response can be divided into three regions.

① Low-frequency region

② Mid-frequency region

③ High-frequency region.

→ The frequency response of any amplifier is a plot between the magnitude of gain and logarithmic frequencies.

Figure (a) shows a frequency response curve of an RC coupled amplifier.

The drop in gain at low-frequency region is due to increase in capacitive reactance. In high frequency region the drop in gain is due to parasitic capacitance.

→ The frequencies corresponding to f_L and f_H are called cut-off frequencies, corner frequency or half power frequency.

$f_L \rightarrow$ Lower cut-off frequency

$f_H \rightarrow$ Higher cut-off frequency.

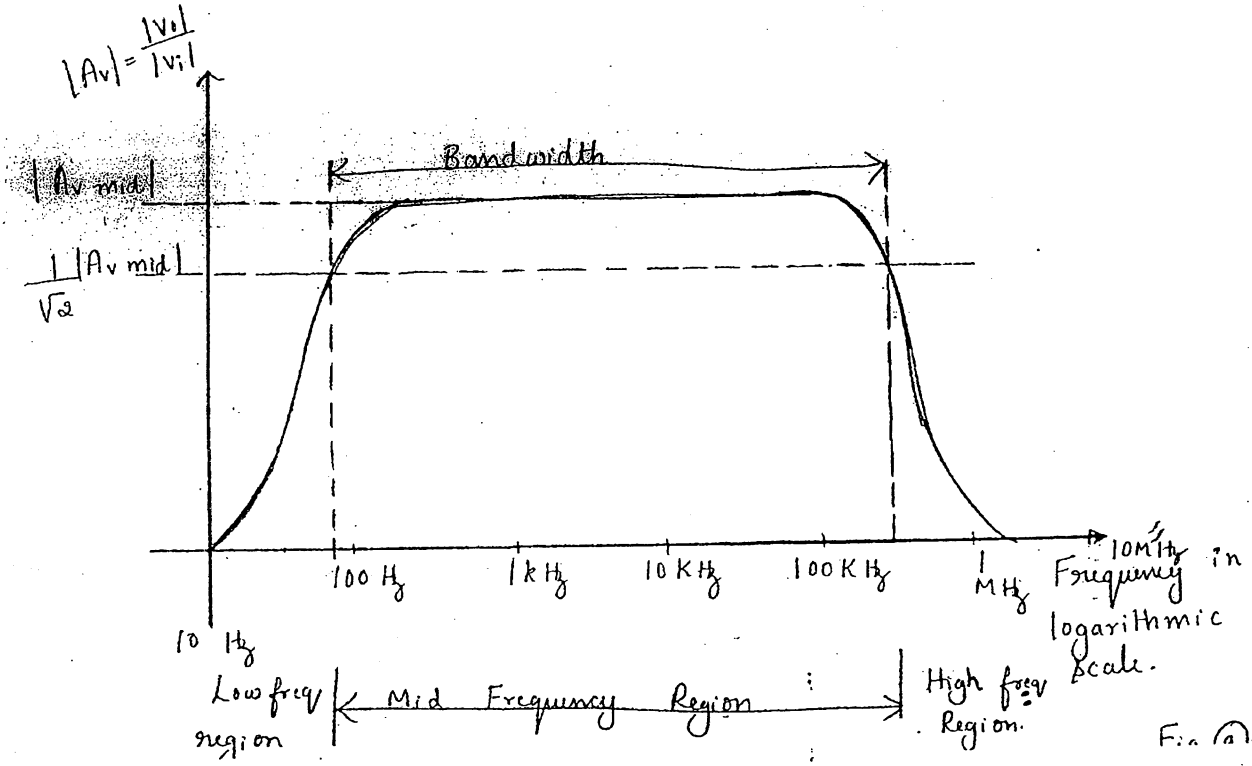


Fig (a).

It is convenient to compare two powers on a logarithmic scale. (2)
The unit of this logarithmic scale is called decibels.

The number N decibels by which a power P_2 exceeds the power P_1 is defined by

$$N = 10 \log_{10} \frac{P_2}{P_1}$$

Negative values of dB means that the power P_2 is less than the reference power P_1 and positive value of dB means that Power P_2 is greater than the reference power P_1.

Advantages of representation of gain in Decibels.

(1) A logarithm changes multiplication to addition, in multistage amplifiers overall gain can be calculated by adding individual gains.

(2) It allows us to denote very large and very small values by considerably small figures.

→ To indicate how constant an amplifiers gain is with frequency variation, the range of frequencies are specified over which the gain does not deviate more than 70.7% of the maximum gain

Although this drop from maximum value to 70.7% may seem to be large drop the change is not easily noticeable, so that an amplifier may be considered to have a flat response in this range of frequencies.

In figure (a) $|A_{v\,mid}|$ indicates the maximum gain of the amplifier.

The power output at mid-frequency is equal to

$$P_{output(mid)} = \frac{|V_o^2|}{R} \longrightarrow (1)$$

The voltage gain at mid-frequency is $= \frac{|V_o|}{|V_i|} \longrightarrow (2)$

using (1) & (2)

$$P_{output(mid)} = \frac{|V_o^2|}{R} = \frac{|A_{v\,mid} V_i|^2}{R}$$

When the gain drops from its max value to 70.7%, the output power is known as half power gain.

$$P_{output-HPF} = \frac{|0.707\, A_{v\,mid}\, V_i|^2}{R} = 0.5 \frac{|A_{v\,mid}\, V_i|}{R}$$

$$P_{output-HPF} = 0.5\, P_{output(mid)}$$

Hence the two frequencies f_L, f_H in figure (a) represent half power points.

The Bandwidth of amplifier can be determined by f_L and f_H and it is expressed by

$$Bandwidth = f_H - f_L$$

This is also called passband of amplifier.

Before the logarithmic plot the magnitude should be normalized. That is the gain at each frequency is divided by midband gain (maximum gain).

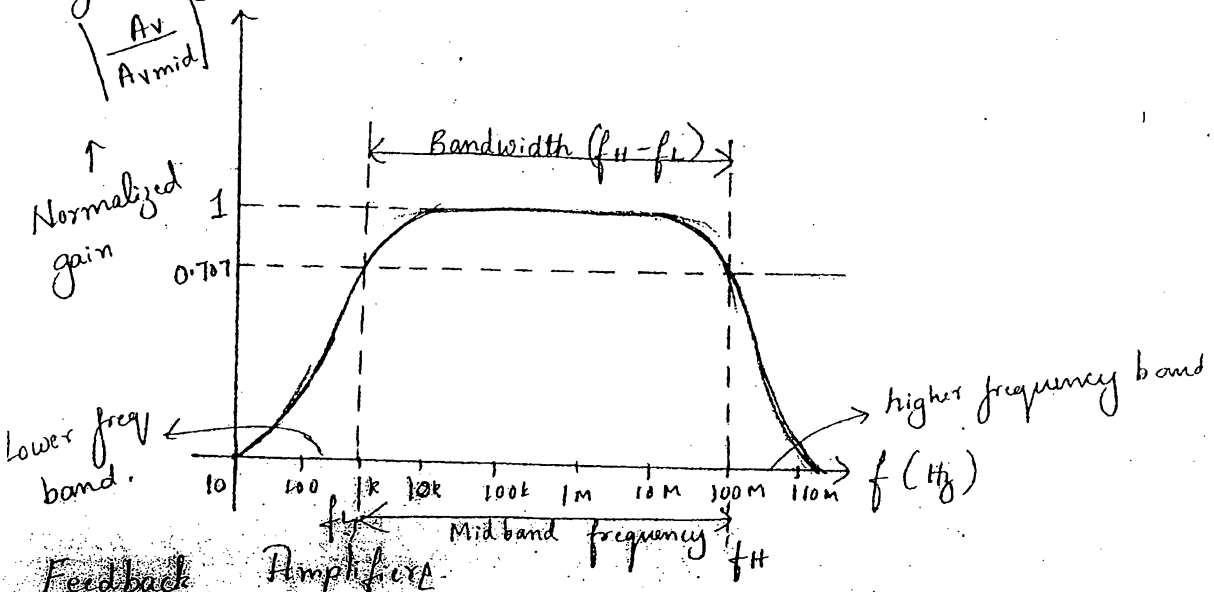
A normalized decibel plot can be obtained by the following (5) transformation.

$$\left.\frac{A_v}{A_{v\,mid}}\right|_{dB} = 20 \log_{10} \frac{A_v}{A_{v\,mid}}$$

The gain at half-power point in decibels is

$$\left.\frac{A_{v\,HPF}}{A_{v\,mid}}\right|_{dB} = 20 \log_{10} \frac{A_{v\,HPF}}{A_{v\,mid}} = 20 \log_{10} \frac{0.707\, A_{v\,mid}}{A_{v\,mid}} = -3\,dB$$

Figure (6) shows the normalized plot of gain versus frequency



Feedback Amplifiers

→ Feedback is a process in which a fraction of the output energy of a system is fed back to its input.

→ Depending on whether the feedback signal aids or opposes the input signal, there are two basic types of feedback in amplifiers.

(1) Positive (Regenerative)

(2) Negative (Degenerative).

Positive feedback : If the signal fed back to the input is in phase with the input signal, it is called positive feedback.

- Positive feedback increases gain of amplifier.
- It also increases distortion and instability of amplifier.
- Positive feedback not used in amplifiers, If positive feedback is sufficiently large, it generates oscillations and hence it is used in oscillators.

Negative Feedback : If the signal fed back to the input is out of phase with the input, it is called negative feedback.

- When used in amplifiers, negative feedback stabilizes the gain.
- It increases the bandwidth and reduces distortions.
- Negative feedback frequently used in amplifiers.

All these desirable properties of amplifiers are obtained at the expense of a reduction in gain.

Feedback Principles.

→ Figure © shows the basic structure of feedback amplifier, it is also known as closed-loop amplifier as feedback forms closed loop between input and output.

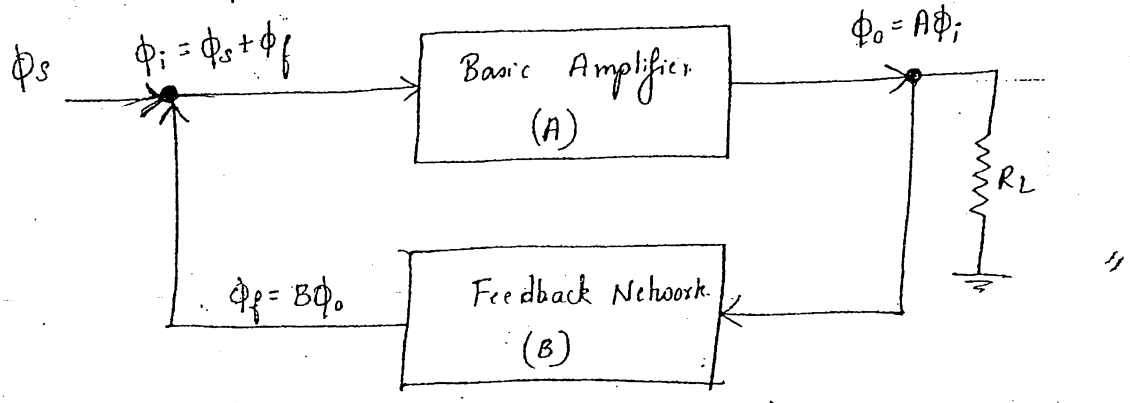


Fig: C Block diagram of feedback amplifiers.

→ Figure c consists of 2 blocks. ↘ amplifier block ↘ feedback block

→ feedback block consists of circuit with active and passive components.

To derive basic feedback equations we assume

Ⓐ Reverse transmission from amplifier output to the input is zero

Ⓐ Forward transmission through the feedback network is zero.

i.e, ideally the signal flows only in certain direction as shown by the arrows.

→ ϕ is the signal quantity (voltage or current)

The gain without feedback is A. Hence without feedback the output ϕ_o is related to the input ϕ_i by

$$\phi_o = A\phi_i$$

→ Consider feedback network, ϕ_o is fed back to the load as well as to the input of feedback network. A fraction of ϕ_o ($B\phi_o$) is fed back to the input and added with externally applied input signal ϕ_s.

The sampled signal → $\phi_f = B\phi_o$

The feedback signal ϕ_f added with external input signal ϕ_s either in phase or in opposite phase to produce input signal ϕ_i

$$\therefore \phi_i = \phi_s + \phi_f = \phi_s + B\phi_o$$

The gain A_f of the feed-back amplifier

$$A_f = \frac{\phi_o}{\phi_s} = \frac{A\phi_i}{\phi_i - B\phi_o} = \frac{A\phi_i}{\phi_i - AB\phi_i}$$

$$\boxed{A_f = \frac{A}{1-AB}}$$ General feedback equation

$AB \rightarrow$ Loop gain or loop transmission function.

$(1-AB) \rightarrow$ Feedback factor.

Positive feedback : If signal ϕ_f is in phase with ϕ_s, feedback is called positive feedback.

$$\phi_i = \phi_s + \phi_f \Rightarrow A_f = \frac{A}{1-AB}$$

* if AB is positive and $AB < 1$ $(1-AB) < 1 \therefore A_f > A$
Thus positive feedback in a controlled manner increases the overall gain of the amplifier

* If $AB = 1$, A_f is infinity. i.e, output signal is available even if ϕ_s is zero. This phenomenon is used in electronic oscillators.

Negative feedback : If signal ϕ_f is out of phase with the input signal ϕ_s, feedback is called negative feedback.

$$\phi_i = \phi_s - \phi_f \Rightarrow A_f = \frac{A}{1+AB}.$$

$$\therefore \quad A_f < A$$

* The gain of feedback amplifier (with negative feedback) is always less than gain of amplifier without feedback.

* If loop gain $AB \gg 1$, $A_f = 1/B$ which means that the gain of feedback amplifier is entirely determined from feedback network. Using suitable feedback network, accurate, predictable

Advantages of Negative Feedback Amplifier

1) Gain Stability

The gain of the amplifier change by environmental change (temperature, humidity), manufacturing tolarance, quiscent point varaiation, ageing of amplifier etc.

The application of negative feedback stabilizes the gain A_f.

We know that for negative feedback amplifier gain

$$A_f = \frac{A}{1+AB} \longrightarrow (1)$$

Differentiate both side w.r.t A, keeping B constant

$$\frac{dA_f}{dA} = \frac{(1+AB)-(A)(B)}{(1+AB)^2} = \frac{1}{(1+AB)^2} \longrightarrow (2)$$

$\div$ both side by A_f

$$\frac{dA_f}{A_f} = \frac{dA}{(1+AB)^2} \times \frac{1}{A_f} = \frac{dA}{(1+AB)^2} \times \frac{1}{\frac{A}{(1+AB)}} \longrightarrow (3)$$

$$\left\langle \frac{dA_f}{A_f} = \frac{1}{(1+AB)} \times \frac{dA}{A} \right\rangle \longrightarrow (4)$$

$\frac{dA_f}{A_f}$ $\longrightarrow$ Fractional changes in the gain with feedback.

$\frac{dA}{A}$ $\longrightarrow$ Fractional changes in the gain without feedback

The ratio of above is Gain desensitivity $S_A = \frac{\partial A_f/A_f}{\partial A/A}$ $\rightarrow (5)$

From equation (4)

$$\frac{dA_f}{A_f} < \frac{dA}{A}$$

Thus. percentage change in A_f is smaller than the percentage change in A by an amount of feedback factor $(1+AB)$.

Eg: Let amplifier open loop gain $A=200$

The feedback fraction $B=0.1$

If the open loop gain (A) changes by 10%. i.e, $\frac{dA}{A} \times 100 = 10\%$ due to temperature

then percentage change in closed loop gain is

$$\frac{dA_f}{A_f} = \frac{1}{(1+0.1\times200)} \times 10\% = 0.4761 \approx \underline{0.5\%}$$

---

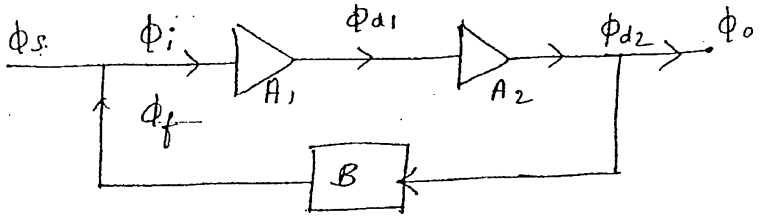
(2) Noise Reduction

The sources of noise may be power supply ripple voltage, non-linearity of active devices, power supply hum (audio power amplifiers) and other disturbances.

Any noise introduced at the input of the amplifier is treated like a signal by it and amplifier amplifies. both signal & noise

Lets study the effect of negative feedback on noise or distortion

Consider a two stage amplifier.



Distortion introduced at the output of first as well as second stage amplifier is designated by ϕ_{d1} and ϕ_{d2} respectively.

The output signal ϕ_o can be represented as

$$\phi_o = \frac{\phi_i A_1 A_2}{1 + A_1 A_2 B} + \frac{\phi_{d1} A_2}{1 + A_1 A_2 B} + \frac{\phi_{d2} 1}{1 + A_1 A_2 B}$$

Assuming $|A_1 A_2 B| \gg 1$

$$\phi_0 = \frac{-\phi_{si}}{B} - \frac{\phi_{d1}}{A_1 B} - \frac{\phi_{d2}}{A_1 A_2 B}.$$

The above equation indicates that ϕ_{d2} is reduced by factor $A_1 A_2 B$ and ϕ_{d1} is reduced by $A_1 B$.

Since in most of the amplifiers non-linear distortion is introduced when the signal level is high, the distortion is mainly be contributed by the last stage at the output of amplifier and the noise introduced at the final stage of amplifier is reduced drastically.

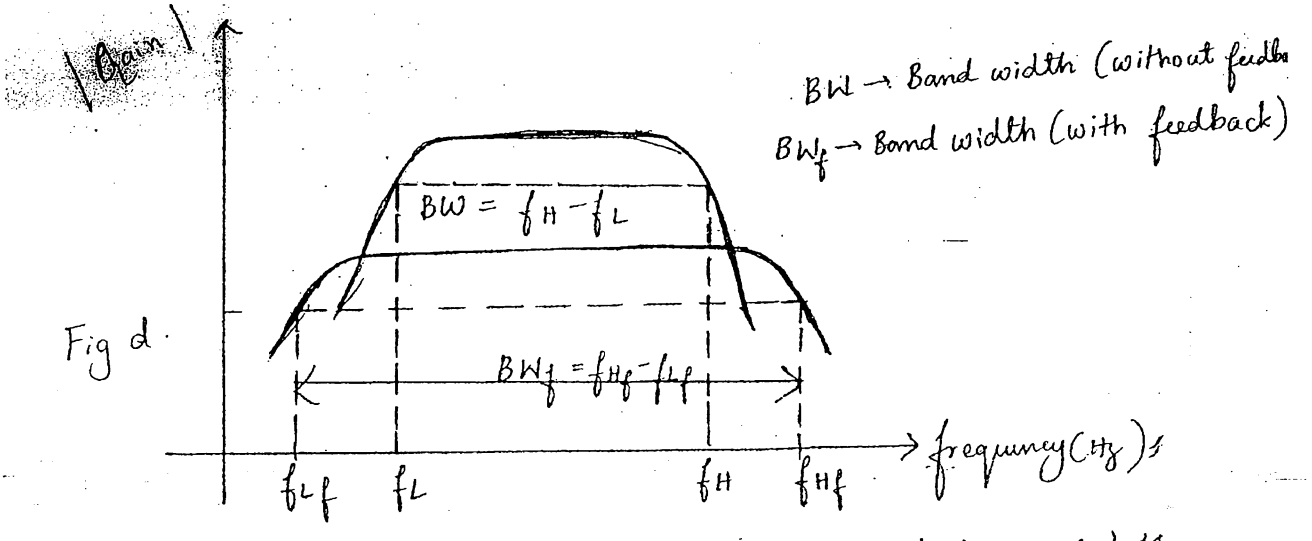
---

(3) Bandwidth Enhancement

For any amplifier, the gain - bandwidth product is always constant.

⟨gain × Bandwidth = Constant⟩

The negative feedback reduces the gain and proportionately increases the bandwidth.



$BW \rightarrow$ Band width (without feedback)
$BW_f \rightarrow$ Band width (with feedback)

Fig d.

In above figure f_H and f_L are upper and Lower cut-off frequencies of an amplifier without feedback and f_{Hf} and f_{Lf} are

) Improvement in Linearity and Signal Handling capacity:

→ The input-output characteristics of an amplifier are called linearity characteristics. Shown in fig (a)
Slope of this curve is called gain of the amplifier.

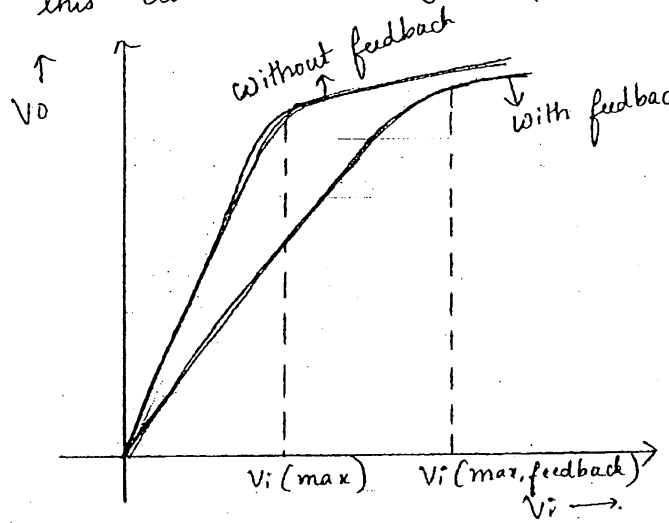


Fig: e

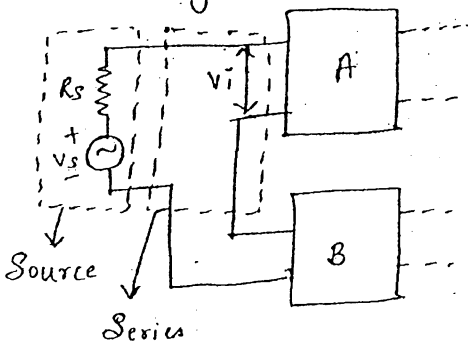
→ The input output characteristics is linear upto maximum input signal level $V_i(max)$ known as signal handling capacity of amplifier. At the input signal level increases beyond this level the output becomes saturated and enters to non linear level.

→ With negative feedback the gain of amplifier decreases consequently slope of linearity characteristic decreases. The signal handling capacity also increases as shown in figure (e)

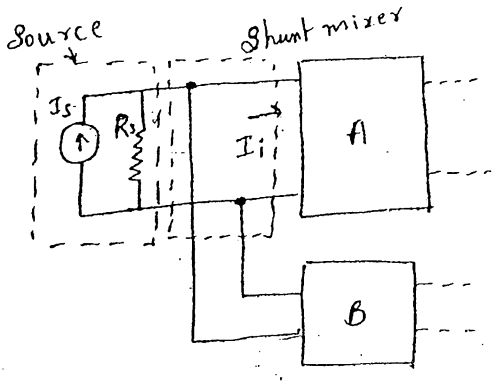
Feedback Amplifier Topologies

In feedback amplifiers, the input signal V_s and the feedback signal V_f are combined in the mixer network to obtain difference signal V_i which is applied as input to the basic amplifier.

There are two types of mixer circuits. series mixing, shunt mixing.

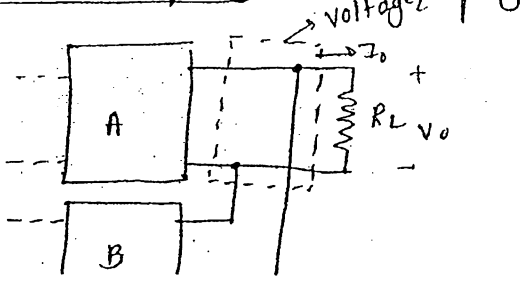


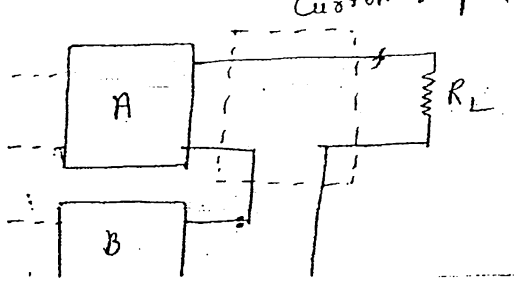
(a) Series Mixing.



(b) Shunt mixing.

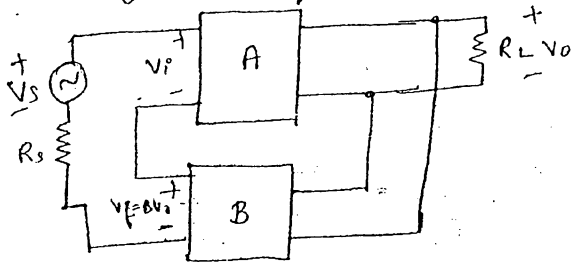
At the output end of feedback amplifier the signal is sampled and given as input to the feedback Network. There are 2 type in sampling network. When output voltage is sampled by connecting the feedback network in shunt across the output, the connection is referred as voltage sampling. Another feedback connection samples the output current and feedback network is connected in series with the output, this is known as current sampling.



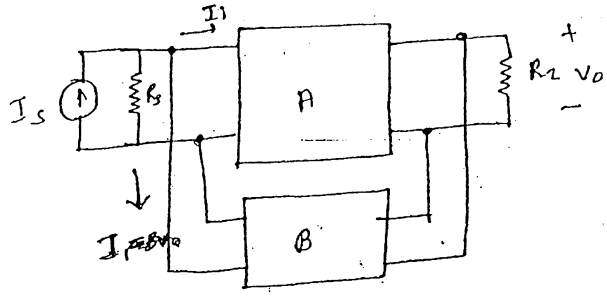


The interconnection of the mixer and sampling network can be either series or in parallel. There are four types of topologies.

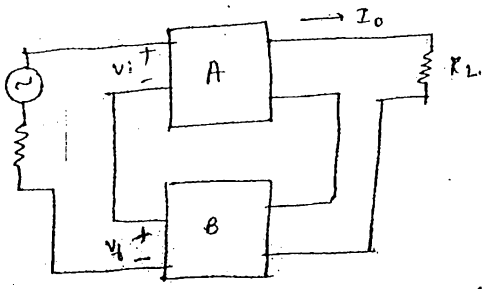
① Voltage series feedback

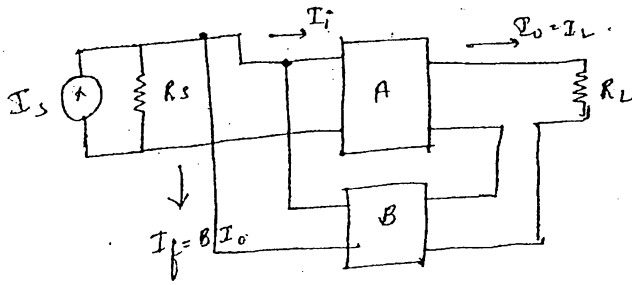


② Voltage - shunt feedback



③ Current Series feedback





Feedback Topology	(Voltage Amplifier) Voltage-series (series-shunt)	(Transimpedance amplifier) Voltage-shunt (shunt-shunt)	(Transconductance Amplifier) Current-series (series-series)	(Current amplifier) Current-shunt (shunt-series)
ain without feedback (A)	V_o/V_i	V_o/i_i	i_o/V_i	i_o/i_i
Feedback function (B)	V_f/V_o	i_f/V_o	V_f/i_o	i_f/i_o
Gain with feedback (Af)	V_o/V_f	V_o/i_s	i_o/V_f	i_o/i_s
) B.W	Increases.	Increases	Increases	Increases
) Noise	Decreases	Decreases	Decreases	Decreases
) Rif	Increases	Decreases	Increases	Decreases

Problems

(1) The voltage amplifier has voltage gain = 300 at cut-off frequencies. Find the maximum voltage gain.

$$\text{Maximum voltage gain} = \text{Gain at cut-off} \times \sqrt{2}$$
$$= 300 \times \sqrt{2}$$
$$\text{Maximum voltage gain} = 424.264.$$

(2) The voltage amplifier has maximum voltage gain of 400. Find the gain at cut-off frequency in dB.

$$\text{The gain at cut off freq} = \frac{\text{Max-gain}}{\sqrt{2}}$$
$$= \frac{400}{\sqrt{2}} = 282.842$$

$$\text{The gain at cut off frequency in dB} = 20 \log_{10}(282.842)$$
$$= \underline{\underline{49.0309 \text{ dB}}}.$$

(or)

$$\text{The maximum gain in dB} = 20 \log_{10}(400) = 52.0412$$

$$\text{The gain at cut off frequency in dB} = 52.0412 - 3$$
$$= \underline{\underline{49.0411 \text{ dB}}}$$

(3) If the higher cut-off frequency of an amplifier = 600 KHz and lower cut-off frequency = 600 Hz. Find the Bandwidth of amplifier.

$$B.W = f_H - f_L = 600 \text{ KHz} - 600 \text{ Hz} = \underline{\underline{599.400 \text{ kHz}}}$$

(4) An amplifier has a B.W of 500 KHz and voltage gain of 100. What should be amount of negative feedback if the B.W is extended to 5 MHz? what will be the new gain after negative feedback is introduced?

Soln: Gain × B.W = Constant $\Rightarrow$ $A_v(BW) = \frac{A_v}{(1+BA_v)}(BW)_f$

$$\left[(BW)_f = (1+B\cdot A_v)(BW)\right]$$

where $(BW)_f \rightarrow$ Bandwidth of amplifier with feedback.

$(BW) \longrightarrow$ Bandwidth of amplifier without feedback.

$B \rightarrow$ The amount of feedback.

$A_v \rightarrow$ The open loop gain of amplifier.

Given

$(BW)_f = 5\ MHz$

$(BW) = 500\ kHz$

$A_v = 100$

$(Bw)_f = (1+B\cdot A_v)(Bw)$

$5\times10^6 = [1+B(100)][500\times10^3]$

$B = 0.09$

The amount of negative feedback, $B = 0.09$.

The gain with feedback $A_f = \frac{A_v}{1+A_vB} = \frac{100}{1+(100)(0.09)}$

$A_f = 10$

---

(5) An amplifier with open-loop voltage gain $A_v = 1000 \pm 100$ is available. It is necessary to have an amplifier whose voltage gain varies by no more than $\pm 0.1\%$.

(a) Find the reverse transmission factor B of the feedback networks used.

(b) Find the gain with feedback.

(a) $$\frac{dA_f}{A_f} = \frac{1}{|1+AB|} \frac{dA}{A}$$

$$\frac{0.1}{100} = \frac{1}{|1+BA|} \frac{100}{1000}$$

$$BA = 99$$

$$B = \frac{99}{1000} = 0.099$$

(b) $$A_f = \frac{A}{1+AB} = \frac{1000}{1+99} = 10$$

Introduction

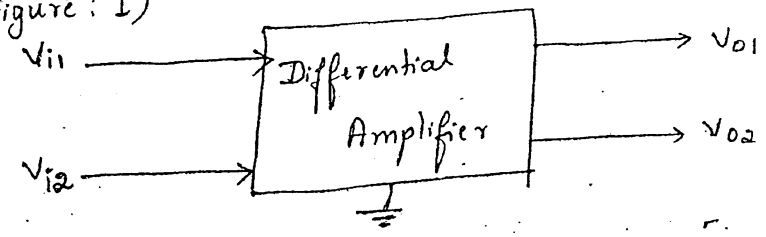
Operational Amplifier (op-amp) is a high gain amplifier. It is used to perform wide variety of Linear and Non-linear functions. Initially this circuit was used to perform different mathematical operations such as addition, subtraction, multiplication, differentiation, integration on input signals. Hence it has been given a name operational amplifier. The early op-amps were bulky, power consuming and expensive as they were using vacuum tubes.

Nowadays integrated (IC) op-amps are very popular as they are inexpensive, take less space, versatile, predictable and flexible. IC version of op-amp uses BJTs and FETs which are fabricated along with some supporting components, on a single semiconductor chip or wafer. Op-amps are system-building blocks in analog electronic circuits. Op-ams are used in the fields of process control, communications, computers, power and signal sources, displays and measuring devices etc.

Differential Amplifiers

The differential amplifier is most widely used circuit building block in analog integrated circuits, it gives high voltage gain.

The block schematic diagram of differential amplifier can be shown as. (Figure : 1)



The differential amplifier has two input terminals V_{i1} and V_{i2} and two output terminals V_{o1} and V_{o2}.

The input and output signals can be applied and measured in different configurations.

dual-input : Two input signals are applied at two input terminals.

single-input : Input is applied to any one terminal (other terminal connected to ground)

Balanced-output : The output voltage is measured between the two output terminals.

Unbalanced-output : The output is measured at one terminal with respect to ground.

Depending on these configurations, various topologies of differential amplifiers are

(i) Dual-input, balanced-output differential amplifier.
(ii) Dual-input, unbalanced-output differential amplifier.
(iii) Single-input, balanced-output differential amplifier.
(iv) Single-input, unbalanced-output differential amplifier.

Op-amp uses dual-input, unbalanced output configuration. Ideally the output is given by

$$V_o = A_d (V_{i1} - V_{i2})$$

$A_d \rightarrow$ Differential gain of amplifier.

The output signal will not only depend on difference of V_{i1} and V_{i2} but it also depends on their average levels.

Hence two signals are defined; difference mode signal V_d and Common mode signal V_c where

$$V_d = V_{i1} - V_{i2} \quad \text{and} \quad V_c = \frac{V_{i1} + V_{i2}}{2}$$

$$V_{i1} = V_c + \frac{V_d}{2}$$

$$V_{i2} = V_c - \frac{V_d}{2}$$

$V_d = V_{i1} - V_{i2}$

$2V_c = V_{i1} + V_{i2}$ (addition)

$2V_{i1} = V_c + 2V_c$

$$V_{i1} = V_c + \frac{V_d}{2}$$

$V_d = V_{i1} - V_{i2}$

$2V_c = V_{i1} + V_{i2}$ (subtract)

$-2V_{i2} = V_d - 2V_c$

$$V_{i2} = V_c - \frac{V_d}{2}$$

Applying the principle of Linear Superpopition theorem, V_o can be expressed in terms of V_d and V_c.

When $V_{i1} \neq 0$ and $V_{i2} = 0$ (Grounded) $V_o = A_1 V_{i1}$

$V_{i1} = 0$ (Grounded) and $V_{i2} \neq 0$ $V_o = A_2 V_{i2}$

Applying superpopition theorem. we can state that

$$V_o = A_1 V_{i1} + A_2 V_{i2}$$

Subplituting expresions for V_{i1} and V_{i2}

$$V_o = A_1 \left(V_c + \frac{V_d}{2}\right) + A_2 \left(V_c - \frac{V_d}{2}\right)$$

$$V_o = A_1 V_c + A_1 \frac{V_d}{2} + A_2 V_c - A_2 \frac{V_d}{2}$$

$$V_o = (A_1 + A_2) V_c + V_d \left(\frac{A_1 - A_2}{2}\right)$$

$$V_o = A_c V_c + A_d V_d$$

Where $A_c = A_1 + A_2 \longrightarrow$ Common mode gain

$A_d = \frac{A_1 - A_2}{2} \longrightarrow$ Differential mode gain.

Differential amplifier is used [illegible]

It is a dc-coupled and avoids large capacitors, which is impractical to realize in IC's. BJT differential amplifier offers a very high-speed logic circuit family called Emitter-Coupled logic (ECL).

→ The simplest form of the differential amplifier is shown below (figure: 2). This circuit is formed by using two matched transistors T_1 and T_2. The emitters of T_1 and T_2 are tied together. This circuit has 2 inputs V_{i1} and V_{i2} and two outputs V_{o1} and V_{o2}.

→ The output voltage V_o is the difference between V_{o1} and V_{o2}. The emitter resistor provides stability and the collector resistor R_c ensures that T_1 and T_2 never enter saturation.

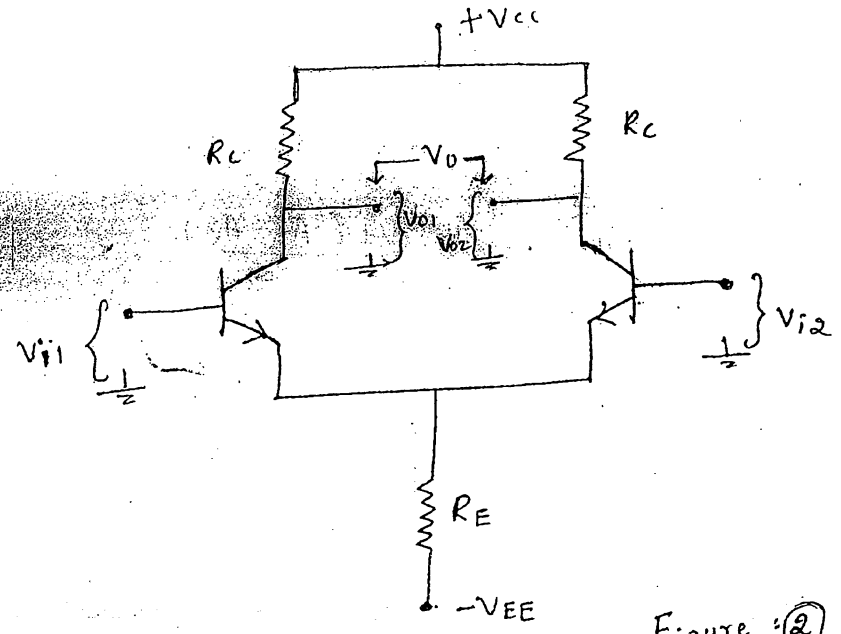


Figure: (2)

Common

When the same signal is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signals appear as a common input signals to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier. In other words, the common mode gain should ideally be zero

The ability of a differential amplifier to reject a common mode signal is defined by its Common-mode Rejection Ratio (CMRR) and it is known as the figure of merit of differential amplifier.

It is expressed as ratio of the differential gain A_d to the common mode gain $\boxed{CMRR = \left|\frac{A_d}{A_c}\right|}$ in dB, $\boxed{CMRR\big|_{dB} = 20\log\left|\frac{A_d}{A_c}\right|}$

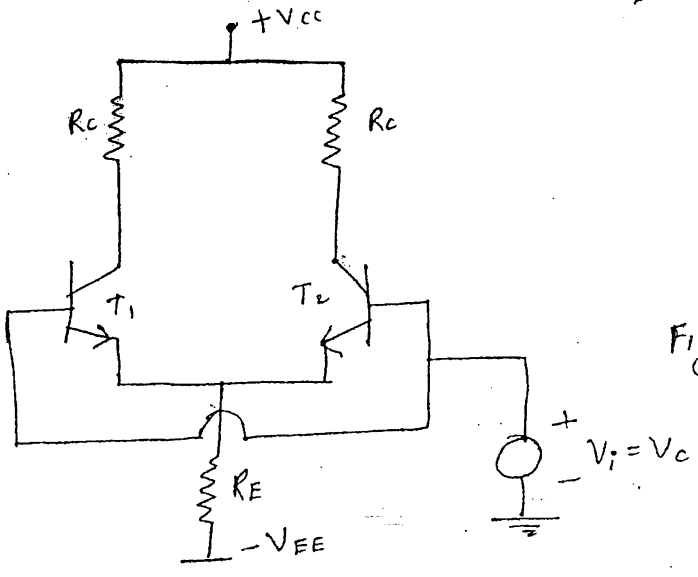


Figure : 3

In ideal case we expect A_c to be zero and the CMRR would be ideally equal to infinity. Thus in practical case it is aimed to design a differential amplifier with higher

Problem.

Determine the output voltage of a differential amplifier for the input voltages of 300μV and 240μV. The differential gain of amplifier is 5000 and the value of CMRR is (i) 100 and (ii) 10^5.

Sol^n

$V_1 = 300\mu V$

$V_2 = 240\mu V$

$A_d = 5000$

$V_o = ?$

$$V_d = V_1 - V_2 = (300 - 240)\mu V = 60\mu V$$

$$V_c = \frac{V_1 + V_2}{2} = \frac{(300 + 240)\mu V}{2} = 270\mu V$$

(i) CMRR = 100

$$CMRR = \frac{A_d}{A_c}$$

$$A_c = \frac{A_d}{CMRR} = \frac{5000}{100} = 50$$

$$V_o = A_c V_c + A_d V_d = (50)(270\mu V) + (5000)(60\mu V)$$

$$V_o = 313.5\,mV$$

(ii) $CMRR = 10^5$

$$A_c = \frac{A_d}{CMRR} = \frac{5000}{10^5} = 0.05$$

$$V_o = A_c V_c + A_d V_d = (0.05)(270\mu V) + (5000)(60\mu V)$$

$$V_o = 300.013\,mV$$

→ An operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals.

→ The op-amps are highly popular due to the fact that its characteristics closely approach the assumed ideal characteristics.

→ As op-amps are built in monolithic ICs, they offer advantages of ICs namely, small size, high reliability, reduced cost and temperature tracking.

Block diagram Representation of a typical op-amp.

→ Commercially available op-amp has four-stage cascaded block structure as shown in figure (4)

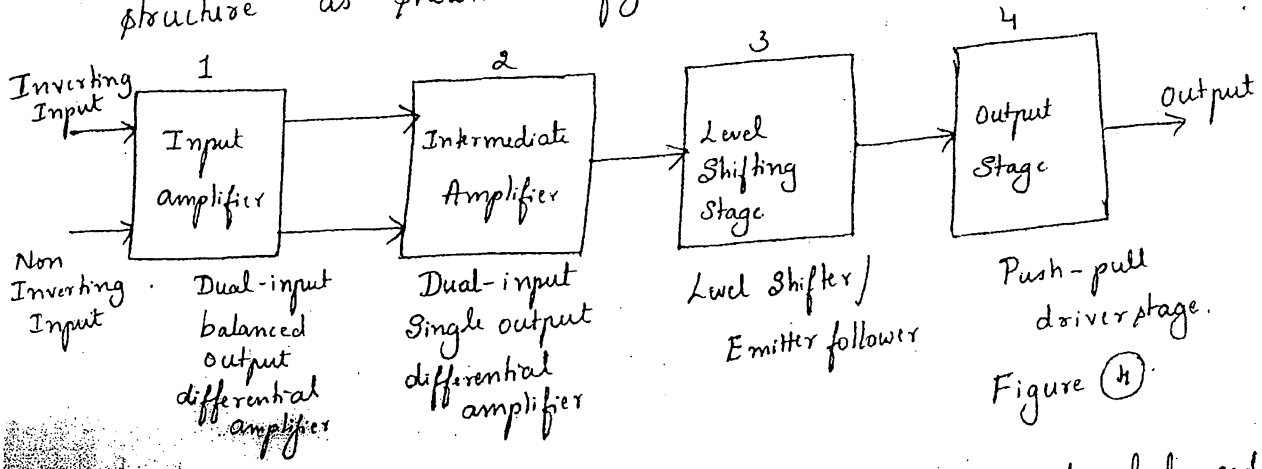


Figure (4)

① Input Amplifier : The first stage is dual input balanced output (double ended) differential amplifier. The input stage of op-amp requires high voltage gain, high input impedance and high CMRR. The differential amplifier used satisfies all these requirements. It provides two input terminals, Inverting input and Non Inverting input.

(2) Intermediate Amplifier

The output of input amplifier is connected as input of next stage (Intermediate amplifier). The main function of intermediate stage is to provide additional gain required, as op-amp requires very high gain.

(3) Level shifting Stage

All stages of amplifier are directly coupled, i.e, capacitors are not used to cascade the stages. Hence op-amp amplifies dc signals also. The dc level increases stage by stage above ground potential. Such high dc level may drive the transistor into saturation. This further causes distortion in the output due to clipping. Hence before output stage it is necessary to bring such a d high dc voltage level to zero with respect to ground. Emitter follower with voltage divider biasing is the simplest level shifter used in op-amp.

(4) Output Stage

The output stage of op-amp requires Large output voltage swing capability, Low output impedance, low power dissipation. The push-pull amplifier satisfies all these requirements. This stage increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground.

The complete op-amp circuit is represented by schematic symbol as shown in figure (5)

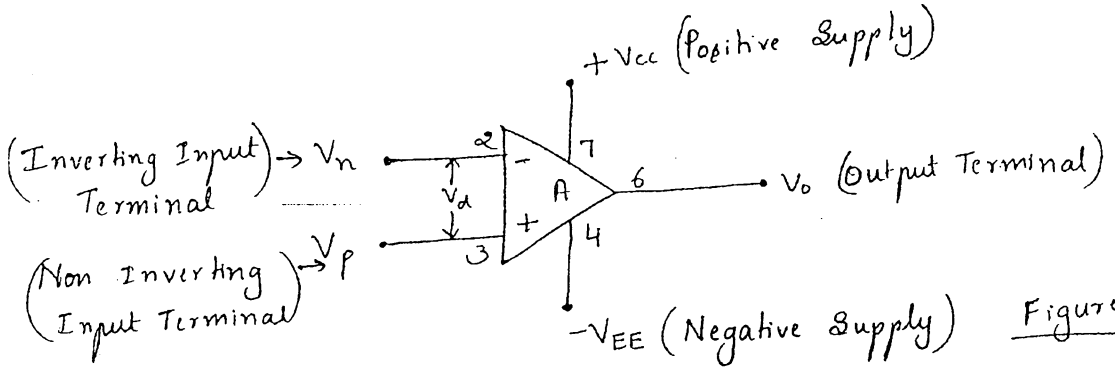


Figure (5)

→ It has one output and two inputs known as inverting and non inverting input designated by (-) and (+) respectively. An ac signal or dc voltage applied to non-inverting input terminal (+) produces an in-phase signal (same polarity) at the output, while the inverting (-) input produces an out-of-phase signal (opposite polarity) at the output. All input and output voltages are measured w.r.t ground.

→ The op-amp works on dual supply. This consists of two supply voltages both d.c. whose middle point is generally the ground terminal.

The dual supply is balanced i.e, the voltages of the positive supply $+V_{CC}$ and that of negative supply $-V_{EE}$ are same in magnitude. If two voltages are not same in dual supply it is called as unbalanced dual supply.

Very popular IC version of op-amp is μA 741. The manufacturer of μA 741 is Fairchild Semiconductor (USA), where μA is Fairchild's own identifying initials. Some other manufacturers are LM, LH, TBA (National Semiconductors), MC, MFC (Motorola), CA, CD, SN (Texas Instruments) etc.

For convenience, widely used op-amp IC is called simply IC 741 op-amp dropping the prefixes.

Figure (6) shows pin diagram of IC 741 op-amp.

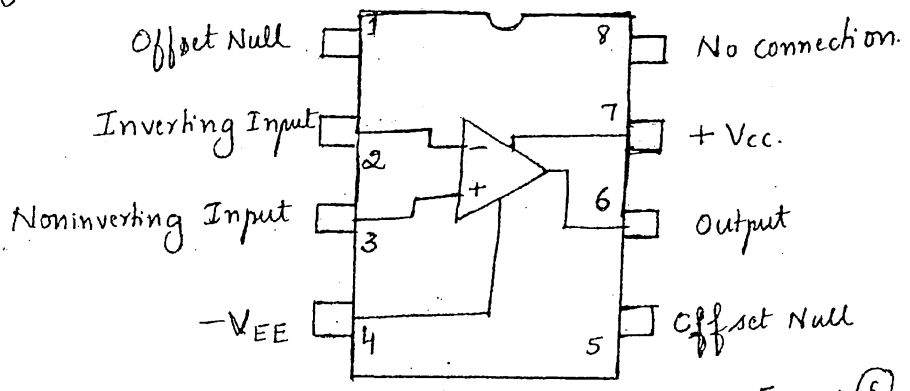


Figure (6)

The pin 2 is inverting input where pin 3 is non inverting input terminal. The output is to be taken from pin 6.

The op-amp requires dual supply, the positive supply is to be given to pin 7 while negative supply is to be given to pin 4.

The Pins 1 and 5 are offset null pins. Ideally, when both the inputs of op-amp are zero, output must be zero. But in practical cases the op-amp produces small output voltage with zero inputs. This voltage existing at the output, when inputs are zero is called output offset voltage. Hence to compensate offset errors pin 1 and 5 are used which

An ideal op-amp would show the following characteristics.

1. Infinite open loop voltage gain ($A_v = \infty$)
2. Infinite input resistance ($R_i = \infty$)
3. Zero output resistance ($R_o = 0$)
4. Infinite Bandwidth ($BW = \infty$)
5. Zero output voltage when input voltage is zero
6. Perfect balance, i.e, zero output voltage when same input voltage is applied at both the inputs.
7. Infinite common mode rejection ratio ($CMRR = \infty$)
8. Infinite slew rate, i.e, output voltage changes simultaneously with input voltage change.
9. Stable characteristics against temperature variation.

A practical op-amp shows following characteristics.

1. Very high voltage gain. ($A_v \approx 2 \times 10^5$)
2. Very high input resistance ($R_i \simeq 2 M\Omega$)
3. Very low output resistance ($R_o \approx 75\Omega$)
4. Very wide bandwidth ($BW \simeq 1 MHz$)
5. Large CMRR. ($CMRR \simeq 90 dB$)
6. Produces small output voltage when input voltage is zero ($\simeq 2m$
7. Slew rate is typically $0.5 V/\mu sec$ at unity gain
8. Produces small output voltages when same input is applied.

Virtual Ground Concept

The analysis of op-amp circuits can be simplified by making 2 assumptions. These assumptions are based on first three ideal op-amp characteristics ($A_v = \infty$, $R_i = \infty$ and $R_o = 0$). These assumptions are also realistic and can be used to obtain the output expression in number of linear applications.

Figure (7) shows the symbol of an ideal op-amp with input voltage and current levels.

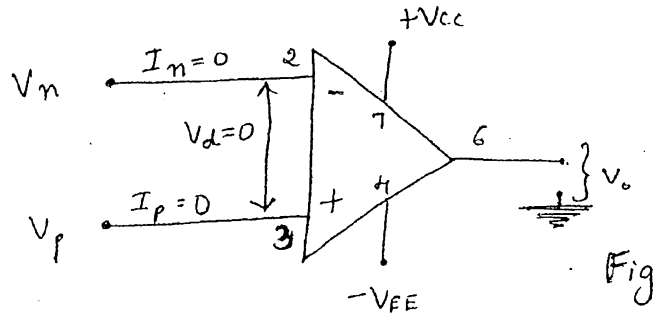


Figure (7)

The input differential voltage between two input terminal is V_d. The output voltage is V_o and I_n and I_p are input currents at inverting and non inverting input terminals.

First we assume that current drawn by either of input terminal (inverting or noninverting) is zero. i.e, $I_n = 0$ and $I_p = 0$. Infinite input impedance means none of the input terminals draw any current.

In practice, the current drawn by the input terminal is very small of the order of μA or nA. Hence the assumption ... current is realistic.