BMS COLLEGE OF ENGINEERING

Bull Temple Road, Bangalore-560019

ELEMENTS OF ELECTRONICS ENGINEERING

SCHEME: UNIT 4

DIGITAL ELECTRONICS

PART-I

1. State and prove De Morgan's law. **(5 marks)**

Ans:

DeMorgan's Theorems:

1. $\overline{A \cdot B} = \overline{A} + \overline{B}$

A	B	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

2. $\overline{A + B} = \overline{A} \cdot \overline{B}$

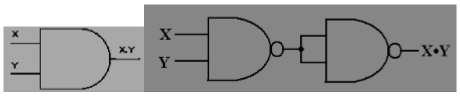
A	B	$A + B$	$\overline{A + B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

2. Discuss the universality of NAND gate. **(5 marks)**

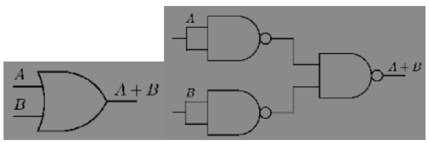
Ans:

NOT gate

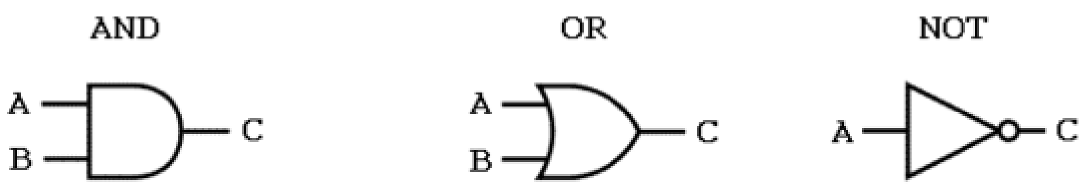
AND gate



OR gate



3. Write the logic symbol and truth table of Basic Gates **(5 marks)**



Ans:

Inputs		Output
A	**B**	**C**
0	0	0
0	1	0
1	0	0
1	1	1

Inputs		Output
A	**B**	**C**
0	0	0
0	1	1
1	0	1
1	1	1

Input	Output
A	**C**
0	1
1	0

4. State and prove duality theorem **(5 marks)**

Ans:

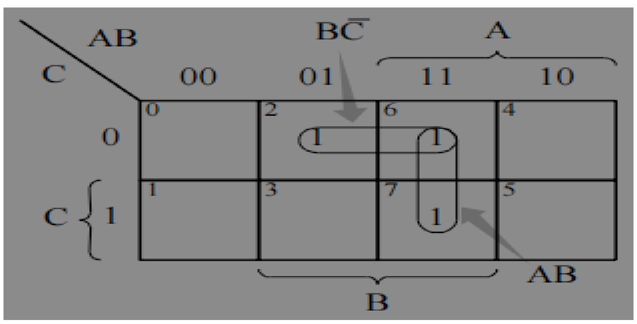
<u>Duality Principle</u>:The duality property of Boolean algebra state that all binary expressions remain valid when following two steps are performed:
Step 1 : Interchange OR and AND operators.
Step 2 : Replace all 1's by 0's and 0's by 1's.
Ex:A(B+C)=AB+AC

- **Dual of the expression is A+(BC)=(A+B)+(A+C)**
- **1.0=0 and its Dual is 0+1=1**

5. Write the steps to reduce expression using K maps for SOP. **(5 marks)**
Ans:

- **An n-variable K-map has 2^n cells with each cell corresponding to an n-variable truth table value.**
- **K-map cells are labeled with the corresponding truth-table row.**
- **K-map cells are arranged such that adjacent cells correspond to truth rows that differ in only one bit position**
- **K-map cells that are physically adjacent are also logically adjacent. Also, cells on an edge of a K-map are logically adjacent to cells on the opposite edge of the map.**
- **If two logically adjacent cells both contain logical 1s, the two cells can be combined to eliminate the variable that has value 1 in one cell's label and value 0 in the other. This is equivalent to the algebraic operation, aP + a′ P =P where P is a product term not containing a or a′.**
- **A group of cells can be combined only if all cells in the group have the same value for some set of variables.**

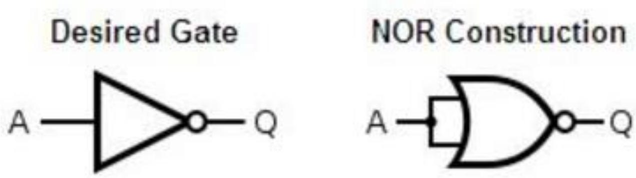
Example: Simplify f= A`BC`+ABC`+ABC



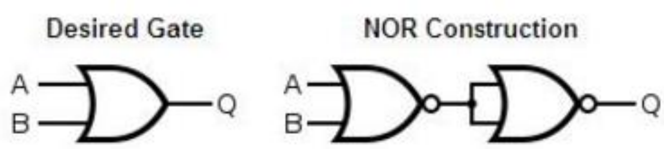
After Simplification: C'B+AB

6. Discuss the universality of NOR gate. (5 marks)
Ans:

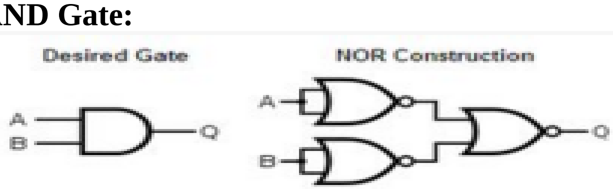
NOT Gate:



OR Gate:



AND Gate:



7. Explain the working of 4x1 multiplexer?

8. Explain the working of 3 to 8 decoder?

9. With truth table explain the working of SR flip-flop?

10. With truth table explain the working of JK flip-flop?

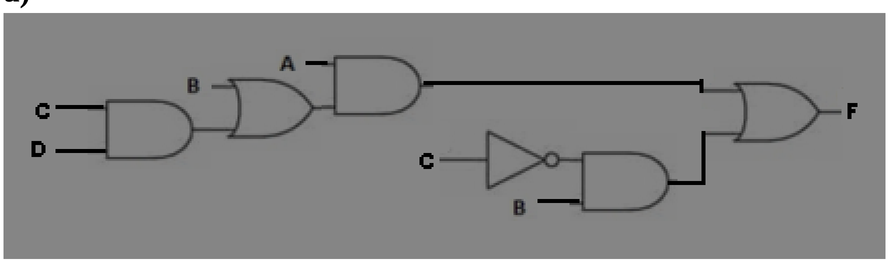
PART-II (APPLY)

1. **Implement the expression F=A(B+CD)+B$\bar{C}$ using** **(10 marks)**

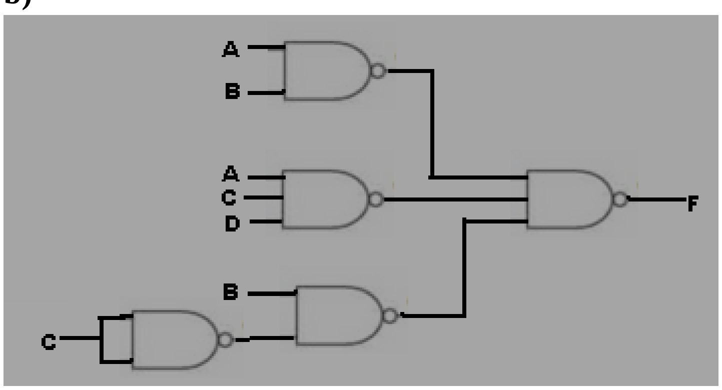
   a)AND –OR -NOTgates
   b) Only NAND gates
   c) Only NOR gates.
   Compare which circuit uses minimum number of gates.

   Ans:

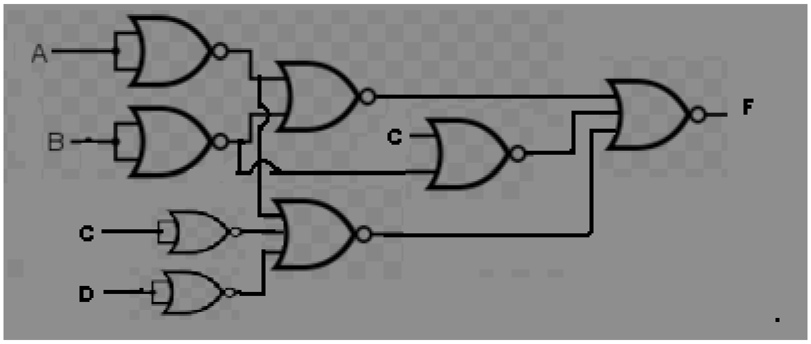
   a)



b)



c)



The expression using only NAND gates uses minimum number of gates-5

2. **Simplify the following Boolean expression using Boolean Laws and Realize using only NAND gates. (10 marks)**

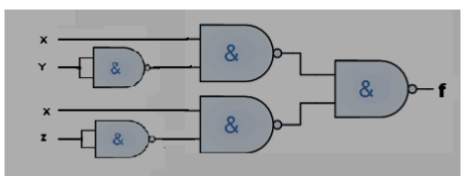
   i) $f(W,X,Y,Z) = \overline{W}XY\overline{Z} + XY\overline{Z} + X\overline{Y}\overline{Z} + X\overline{Y}Z$

   ii) $f(A,B,C) = AB + \overline{A}BC + A\overline{C} + \overline{A}\overline{B}C$

Ans:

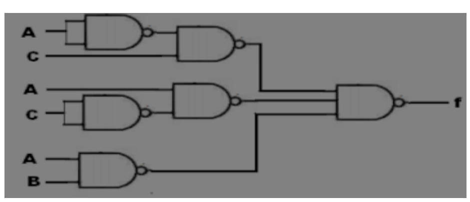
(i) $f(W,X,Y,Z) = \overline{W}XY\overline{Z} + XY\overline{Z} + X\overline{Y}\overline{Z} + X\overline{Y}Z$

$f(W,X,Y,Z) = X\overline{Y} + X\overline{Z}$



(ii) $f(A,B,C) = AB + \overline{A}BC + A\overline{C} + \overline{A}\overline{B}C$

$f(A,B,C) = AB + \overline{A}C + A\overline{C}$



3. **Simplify the following Boolean expression using Boolean Laws and Realize using only NOR gates. (10 marks)**

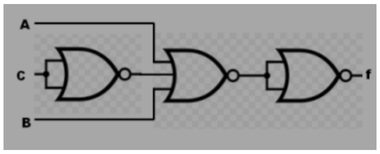
   i) $f(A,B,C) = A\overline{B}\,C + \overline{C} + BC$

   ii) $f(A,B,C) = \overline{AB} + \overline{B} + \overline{CA}$

Ans:

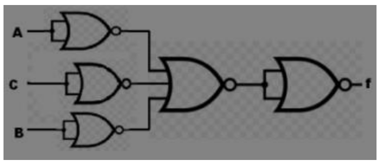
(i) $f(A,B,C) = A\overline{B}\,C + \overline{C} + BC$

$f(A,B,C) = A + \bar{C} + B$



(ii) $f(A,B,C) = \overline{AB} + \overline{B} + \overline{CA}$

$f(A,B,C) = \bar{A} + \bar{B} + \bar{C}$

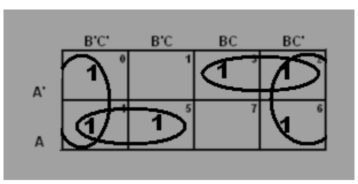


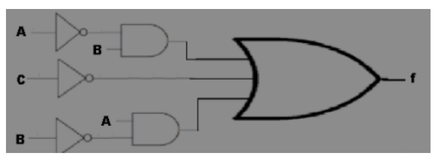
4. **Simplify the following using K-map and realize using minimum number of Basic gates.**
   - **(i)** $f(A,B,C) = \sum m(0,2,3,4,5,6)$ **(10 marks)**
   - **(ii)** **Y (A, B, C) =∑m (0, 1, 5, 7)**
   - **(iii)** **f(x,y,z) = Σm(0,1,3,4,5,7) using K-map**

Ans:

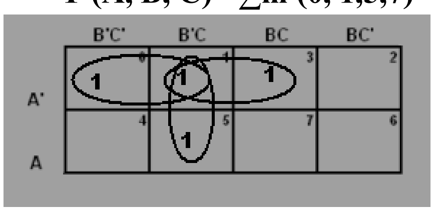
(i) $f(A,B,C) = \sum m(0,2,3,4,5,6)$

$f(A,B,C) = A\bar{B} + \bar{C} + B\bar{A}$

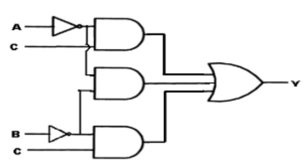




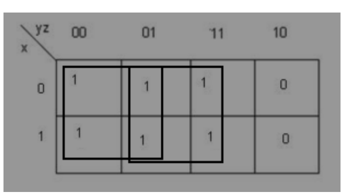
ii) **Y (A, B, C) =∑m (0, 1,5,7)**



$f(A,B,C) = \bar{B}\,C + \bar{A}C + \bar{B}\bar{A}$



iii)f(x,y,z) = Σm(0,1,3,4,5,7) using K-map



$f(X,Y,Z) = \bar{Y} + Z$

5. **Simplify and realize using only 2 input NOR gates.** **(10 marks)**

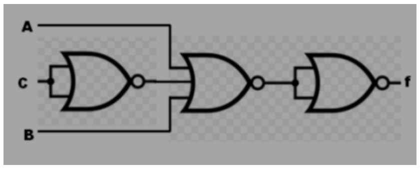
(i)$f(A,B,C) = A\bar{B}\,C + \bar{C} + BCA + BC$

(ii) $f(A,B,C) = \overline{AB} + \bar{B} + \overline{CA} + \bar{B}\bar{C}$

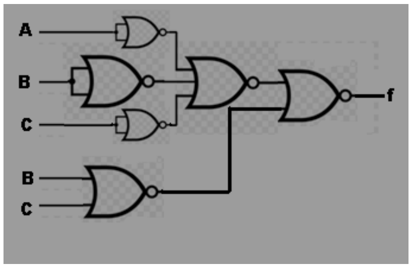
Ans:

(i)$f(A,B,C) = A\bar{B}\,C + \bar{C} + BCA + BC$

$$f(A,B,C) = A + \bar{C} + B$$



(ii) $f(A,B,C) = \overline{AB} + \bar{B} + \overline{CA} + \bar{B}\bar{C}$



$$f(A,B,C) = \bar{B}\bar{C} + BCA$$

6. **If the variables A, B and C can take only the values 0 and 1, prove the following identities of Boolean algebra** **(10 marks)**

i)$\bar{X}\bar{Y}Z + \bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} = \bar{X}(\bar{Y} + \bar{Z})$

ii)$\bar{A}B\bar{C} + B\overline{CD} + AD = AD + B\bar{C} + B\bar{D}$

Ans:

i) $\bar{X}\bar{Y}Z + \bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} = \bar{X}(\bar{Y} + \bar{Z})$

$LHS = \bar{X}\bar{Y}Z + \bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z}$

$= \bar{X}\bar{Y} + \bar{X}Y\bar{Z}$

$= \bar{X}(\bar{Y} + Y\bar{Z})$

$= \bar{X}(\bar{Y} + \bar{Z})$

= RHS

ii) $\bar{A}B\bar{C} + B\overline{CD} + AD = AD + B\bar{C} + B\bar{D}$

$LHS = \bar{A}B\bar{C} + B\overline{CD} + AD$

$= \bar{A}B\bar{C} + B(\bar{C} + \bar{D}) + AD$

$= B\bar{C}(\bar{A} + 1) + B\bar{D} + AD$

$= B\bar{C} + B\bar{D} + AD$

= RHS

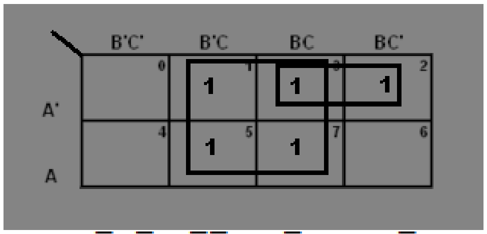
7. **Simplify the following functions by K map method** **(10 marks)**

i)$F = \bar{A}B + \bar{A}C + BC + A\bar{B}C$

ii)$F = \bar{A}B\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C$

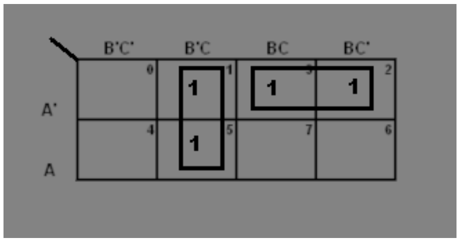
Ans:

i) $F = \bar{A}B + \bar{A}C + BC + A\bar{B}C$



$F = \bar{A}B + C$

ii) $F = \bar{A}B\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C$

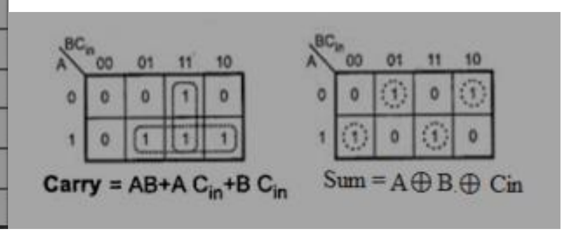


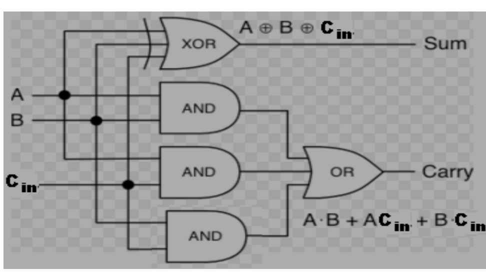
$F = \bar{A}B + \bar{B}C$

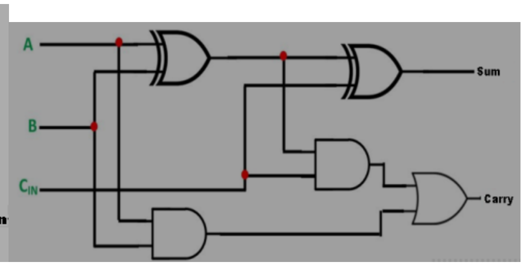
14. Write the truth table and gate level logic diagram for the full adder, realize the same using Half adders (10 marks)

Ans:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



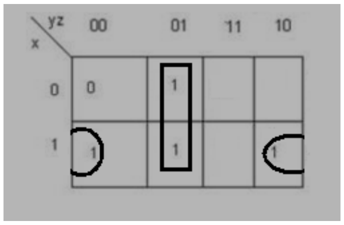




8. **Simplify the following functions by K map method (10 marks)**
   i) $F = xy' + x'y'z + xyz'$
   ii) X = a'b'c' + a'bc' + a'bc + ab'c + abc'

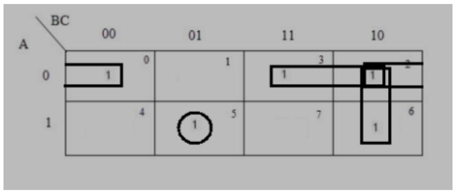
Ans:

i) $F = xy' + x'y'z + xyz'$



$F = y'z + xz'$

ii) **X = a'b'c' + a'bc' + a'bc + ab'c + abc'**



X = a'c' + a'b + ab'c + bc'

9. If the variables A, B and C can take only the values 0 and 1, prove the following identities of Boolean algebra **(10 marks)**

i) $\bar{A}BC + A\bar{B}\bar{C} + ABC + AB\bar{C} = BC + A\bar{C}$

ii) AB+C($\overline{A \odot B}$)= AB+BC+CA

Ans:

i). $\bar{A}BC + A\bar{B}\bar{C} + ABC + AB\bar{C} = BC + A\bar{C}$

$RHS = BC(\bar{A} + A) + (\bar{B} + B)A\bar{C}$

$= BC + A\bar{C} = LHS$

ii). AB+C($\overline{A \odot B}$)= AB+BC+CA

$RHS = AB + BC + AC$

$= AB + BC(A + \bar{A}) + AC(B + \bar{B})$

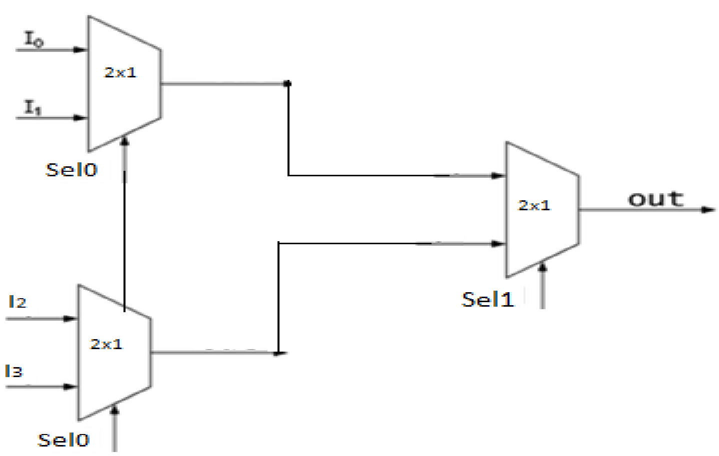
$= AB(1 + C + C) + C(\bar{A}B + A\bar{B})$

$= AB + C(\bar{A}B + A\bar{B})$

$= AB + C(\bar{A}B + A\bar{B}) = AB + C(\overline{A \odot B})$

$= LHS$

10. Implement a 4x1 mux using 2x1 mux. explain the concept.



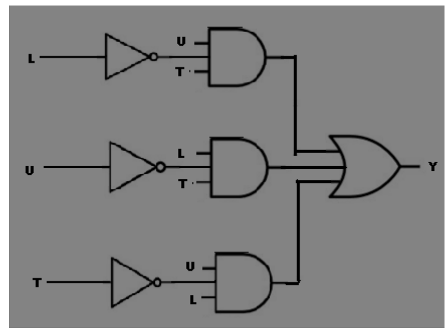
Part III (Analyse, Design, Questions from GATE)

1. The rocket motor of an air-launched missile with three inputs (launch, Unsafe- height and target-lock), will operate if and only if any two inputs are high. Design a suitable logic circuit with minimum logic gates (5 marks)

Ans:

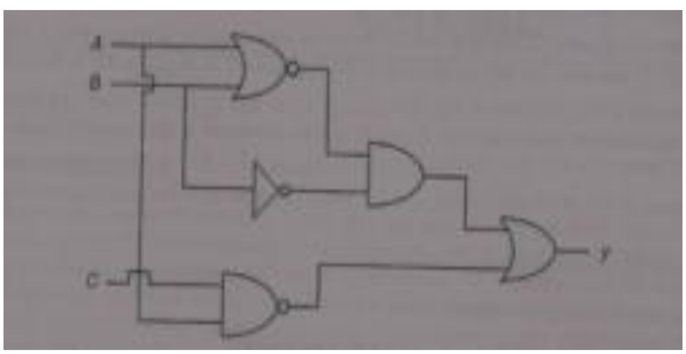
Launch(L)	Unsafe Height(U)	Target Lock(T)	Output(Y)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Y=$\bar{L}UT + LT\bar{U} + LU\bar{T}$



2.Analyze the logic circuit shown in fig. Determine the Boolean function for y and state its truth table. (5 marks)

Ans:



Y=$((\overline{A+B}).\bar{B}) + \overline{AC}$

Y=$\bar{A} + \bar{C}$

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

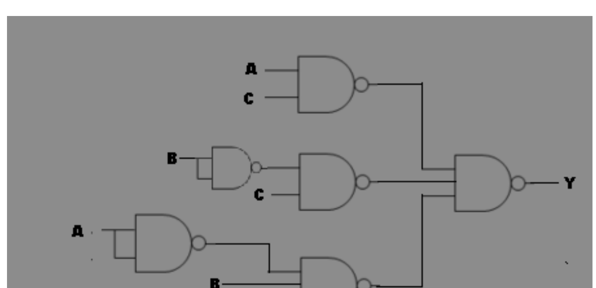
3. A logic circuit has 3 inputs A, B, C and one output Y. Y=B XOR C when A=0, and Y=C when A=1. Simplify the output expression and realize the same using only NAND gates.

(5 marks)

Ans:

A	B	C	Y
0	0	0	0

Y=$\bar{B}C + AC + \bar{A}B\bar{C}$

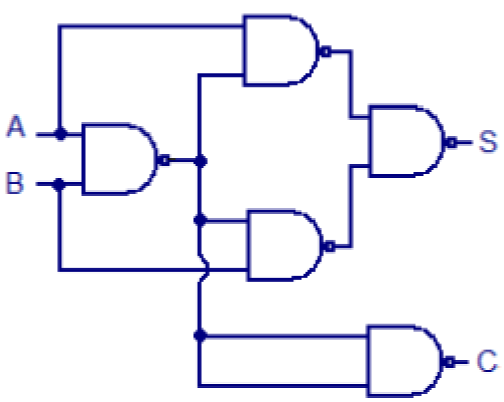


0	**0**	**1**	**1**
0	**1**	**0**	**1**
0	**1**	**1**	**0**
1	**0**	**0**	**0**
1	**0**	**1**	**1**
1	**1**	**0**	**0**
1	**1**	**1**	**1**

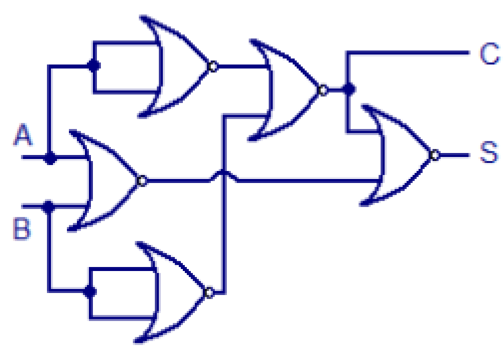
4. Design a two input adder using only NAND gates **(5 marks)**
Ans:

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = A \oplus B$ $C = AB$



Half adder using NAND logic



Half adder using NOR logic

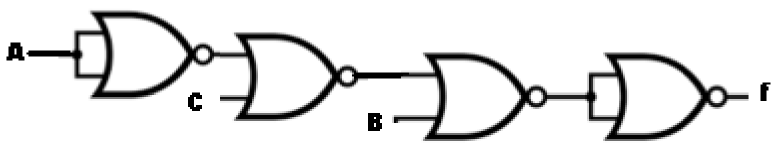
5. Design a logic circuit using minimum number of NOR gates to implement the followingexpression. **(5 marks)**

Ans:

$$f(A,B,C) = \bar{A}B + B\bar{C} + BC + A\bar{B}\bar{C}$$

$$f(A,B,C) = B(\bar{A} + \bar{C} + C) + A\bar{B}\bar{C}$$

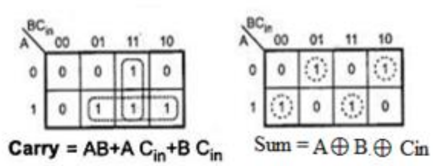
$$f(A,B,C) = B + A\bar{C}$$

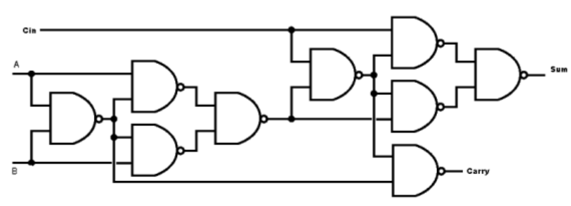


6. Design a combinational circuit to realize a full adder using only NAND gates. (5 marks)

Ans:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



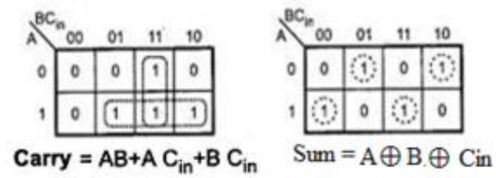


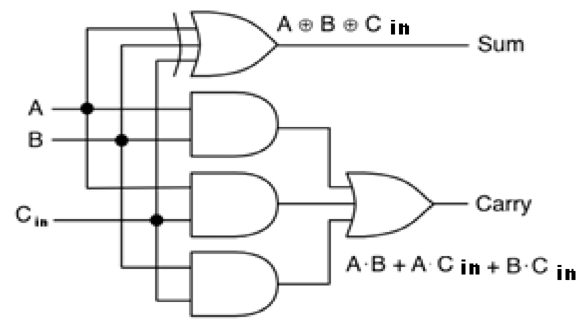
Full-Adder circuit using NAND gates

7.Design a combinational circuit to implement full adder using logic gates. (5marks)

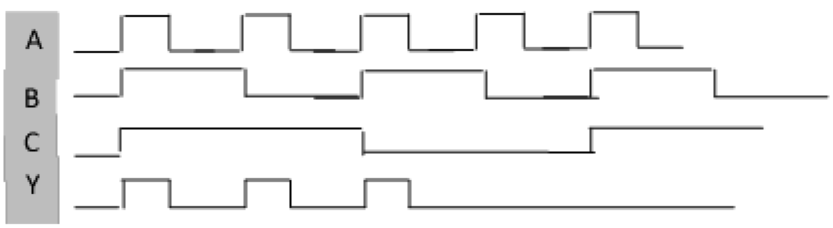
Ans:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1





8.Analyze input and output waveforms shown in Figure 2 and write the truth table.(5 marks)



Inputs			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

9. Design a circuit that has three bit binary input and a single output(Z) specified as follows:

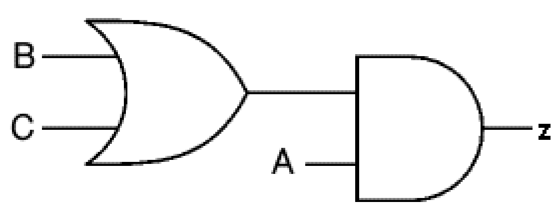
- **Z = 0 ; when the input is less than $(5)_{10}$**
- **Z = 1 ; otherwise**

Ans:

Z=AC+AB

or Z=A(C+B)

Inputs			Output
A	B	C	Z
0	0	0	0
0	0	1	0



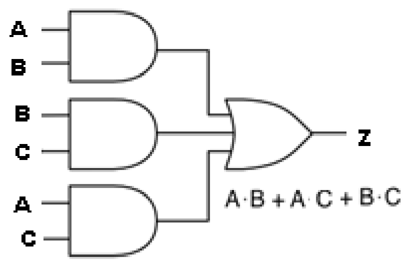
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

10. A bank locker consists of three keys; the locker will get open if any 2 keys are correctly inserted. Design a digital circuit for this scenario. (5 marks)

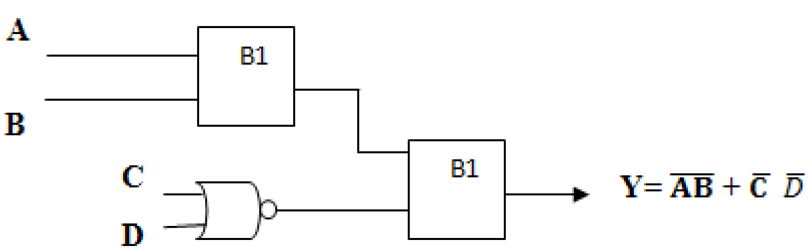
Ans:

Inputs			Output
A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

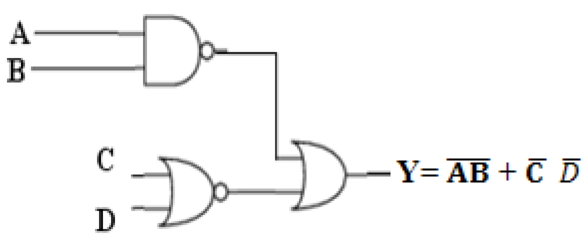
Z=AB+BC+AC



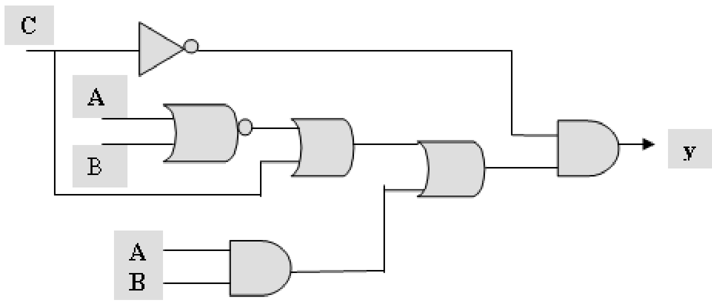
11. Analyze the given circuit to identify the logic used in the blocks B1 and B2 to obtain output Y. (5 marks)



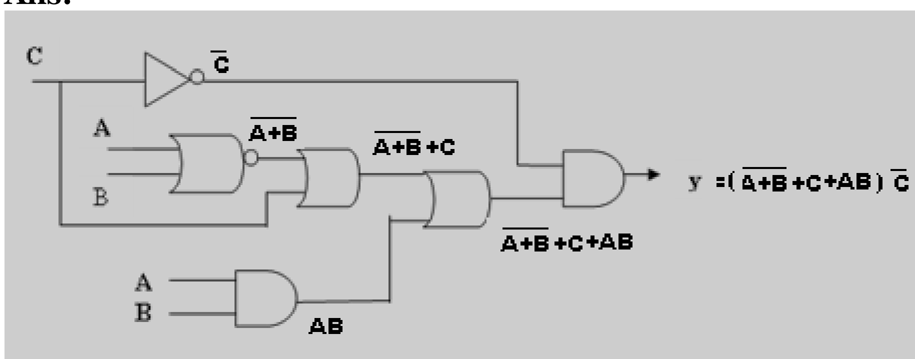
Ans:



12. Analyze the below given logic circuit for an output Y when input C=0. Write expression at each stage (5 marks)



Ans:



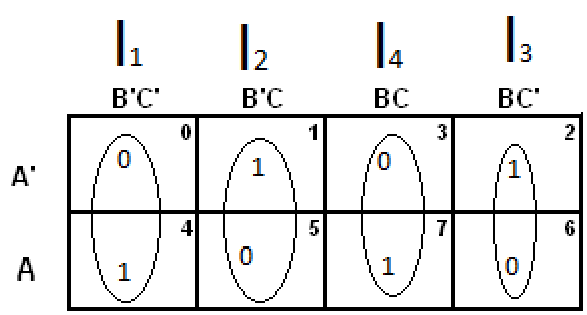
Given C=0, y=$\overline{A}.\overline{B} + AB$

13. Design a Full adder using 4x1 mux.

For sum output : input B and C acts as select lines, as per the truth table of 4x1 mux output fallows: I_1 when BC=00, I_2 when BC=01, I_3 when BC=10 and I_4 when BC=11.

Truth table :

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



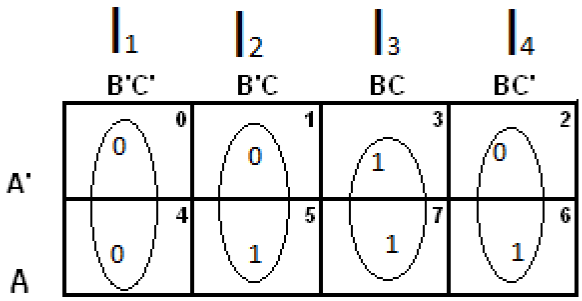
From the K-map expression for 4 inputs of the MUX can be written as

I_1 = A I_2 = A' I_3 = A' I_4 = A

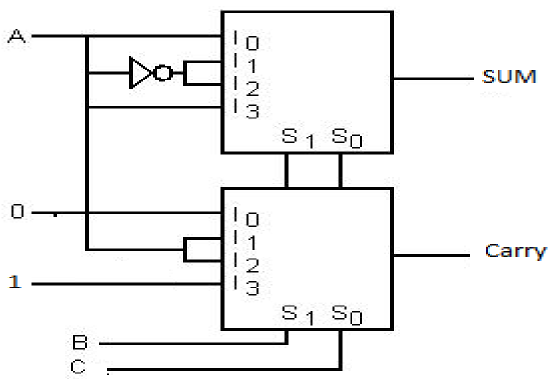
For Carry output:

From the K-map expression for 4 inputs of the MUX can be written as

I_1 = 0 I_2 =A I_3 = 1 I_4 = A



Logic diagram for the full adder using 2 4X1 mux:



14. Design a full adder using 3 to 8 decoder.

Truth table :

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL ADDER

Expressions:

Equation for sum

S = ab'c' + a'b'c + a'bc' + abc

= Σ(1,2,4,7)

Equation for carry

C_{out}= ab + ac + bc

= abc +a'bc +ab'c+abc'

= Σ (3, 5, 6, 7)

So we can implement it from decoder using OR gates as follow: