U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

February / March 2023 Semester End Main Examinations

Programme: B.E. **Semester: V**
Branch: Electrical & Electronics Engineering **Duration: 3 hrs.**
Course Code: 19EE5PE1DS **Max Marks: 100**
Course: DIGITAL SYSTEM DESIGN USING VERILOG **Date: 03.03.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) With truth tables, explain the following Verilog primitives: **06**

i)bufif0 (ii) nor (iii)xor

b) In the Verilog code, find the values of f1, f2 and f3; **06**

```
wire [7:0] a, b, c; wire f1, f2, f3;
assign a=4'b0111;
assign b=4'b1100;
assign c=4'b0100;
assign f1= ^ a;
assign f2= &(a^b);
assign f3=^a&~ ^b;
```

c) With an example differentiate the following. **08**
i. Nets and Register
ii. Inertial and propagation delay

UNIT - II

2 a) Using Verilog gate-primitives, develop a Verilog structural model for the 4:1 multiplexer (with "a" as 4 bit input "sel" as selection lines and y as output). Design 16:1 multiplexer (with "a" as 16-bit input "sel" as selection lines and y as output) using 4:1 multiplexer and write Verilog code for same. **10**

b) Design and write VERILOG code to implement the functionality of 1-bit Full Adder using Data flow modeling. **10**

OR

3 a) Design 2:4 decoder where "en" as enable input, "i" as 2-bit input and "y" as 4-bit output of decoder. Write a Verilog code for the same using case statement. Design 4:16 decoder using 2:4 decoder and write Verilog code for same. **10**

b) Design and write VERILOG code to implement the functionality of Carry Look Ahead Adder. **10**

UNIT - III

4	a)	Write a behavioral model for a universal shift register with the following specification: active low synchronous reset input (clrb) that resets all flip flops. Two control inputs (S1S0) when 00, no action, when 10, register is shifted right and serial data SDR enters Q0, when 01, 4 bit data shifted left and SDL enters Q3. If S1S0=11, 4 bit data (D) is loaded parallel.	**07**
	b)	Write a Verilog behavioral code for mod-12 counter with input as CLK and asynchronous active low reset and output as Q3-Q0.	**06**
	c)	Explain the following control statement with an example. i) if……else statement ii)for loop	**07**

OR

5	a)	Discuss sequential and parallel blocks with examples for each.	**05**
	b)	Design and write VERILOG codes to implement the functionality for i) JK Flip Flop ii) D Flipflop.	**10**
	c)	What is a testbench? What does $display, $monitor, $stop and $finish statements specify in a testbench?	**05**

UNIT - IV

6	a)	Write a Verilog code for the "101" sequence detector using Mealy model without overlapping is realized.	**10**
	b)	Design and write VERILOG code to implement the functionality of 4 bit Gray code to Binary code convertor.	**10**

UNIT - V

7	a)	Compare the following: Programmable Logic Array and Programmable Array Logic.	**06**
	b)	Implement the following Boolean expression with the help of programmable logic array. X=AB+AC' Y=AB'+BC+AC'	**08**
	c)	Write the comparison of FPGA and ASICs.	**06**

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