U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

January / February 2025 Semester End Main Examinations

Programme: B.E. **Semester: V**

Branch: Electrical and Electronics Engineering **Duration: 3 hrs.**

Course Code: 23EE5PE1DS **Max Marks: 100**

Course: Digital system design using Verilog

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

		UNIT - I	CO	PO	Marks
1	a)	Explain the different design methodologies employed in Verilog. Give their merits and demerits	CO1	PO1	**06**
	b)	What are the different data types available in Verilog?	CO1	PO1	**08**
	c)	Given X=4'b1011,Y=4'b1001 and Z=4'b1110,then the output of the following statements are: 1. X | Z 2. &Y 3. ~^ Z 4. X>>2 5. {X, {2{2'b10}}}	CO1	PO1	**06**
		OR			
2	a)	Depict the typical ASIC design flow with the help of appropriate flow diagram.	CO1	PO1	**06**
	b)	What are the different data operators available in Verilog?	CO1	PO1	**08**
	c)	For the following Verilog code segment: wire[7 : 0] A; wire B; assign B = ^A; if the value of A is 8'b 10110011, What will be the value of {A[4:3], 3 {B}}?	CO1	PO1	**06**
		UNIT - II			
3	a)	Use structural modeling to design and write a Verilog code to implement a 3-bit magnitude comparator taking appropriate instances of full adders.	CO3	PO3	**10**

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<table>
<tr><td></td><td></td><td>b)</td><td>Using generate statements, write a Verilog code for an n-bit ripple carry adder.</td><td>CO3</td><td>PO3</td><td>10</td></tr>
<tr><td></td><td></td><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td></td><td>4</td><td>a)</td><td>Use structural modeling to Write Verilog code to implement the functionality of Master –Slave JK Flip flop</td><td>CO3</td><td>PO3</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Write a data flow model for 2:4 Decoder with an active low enable E and an active low output line w.</td><td>CO3</td><td>PO3</td><td>10</td></tr>
<tr><td></td><td></td><td></td><td>UNIT - III</td><td></td><td></td><td></td></tr>
<tr><td></td><td>5</td><td>a)</td><td>Design and also Write a Verilog behavioural code to implement a BCD Adder.</td><td>CO3</td><td>PO3</td><td>06</td></tr>
<tr><td></td><td></td><td>b)</td><td>With relevant examples, bring out the difference between
i) Blocking and non- blocking statements
ii) Initial and always blocks</td><td>CO3</td><td>PO3</td><td>06</td></tr>
<tr><td></td><td></td><td>c)</td><td>Write a behavioural code to represent the functionality of a n-bit shift register having a serial input data D, parallel data P and active high clock input.</td><td>CO3</td><td>PO3</td><td>08</td></tr>
<tr><td></td><td></td><td></td><td>OR</td><td></td><td></td><td></td></tr>
<tr><td></td><td>6</td><td>a)</td><td>Develop a Verilog code to realize the functionality of a 4:16 decoder having an enable En, data input w, using 2:4 decoders.</td><td>CO3</td><td>PO3</td><td>06</td></tr>
<tr><td></td><td></td><td>b)</td><td>Design and develop a behavioural Verilog code to implement the functionality of a 3-bit synchronous Down counter.</td><td>CO3</td><td>PO3</td><td>06</td></tr>
<tr><td></td><td></td><td>c)</td><td>Write a hierarchial code that can perform shift operation of a 4-bit data in parallel / serial fashion. Use multiplexers.</td><td>CO3</td><td>PO3</td><td>08</td></tr>
<tr><td></td><td></td><td></td><td>UNIT - IV</td><td></td><td></td><td></td></tr>
<tr><td></td><td>7</td><td>a)</td><td>Develop a state diagram, state assigned table represented by the following state table. Use T flip flops for FF-2 and D flip flops for FF1. Also write a Verilog code.
<table>
<tr><td>PS</td><td colspan="2">NS
w=0 w=1</td><td>Output</td></tr>
<tr><td>y_2y_1</td><td colspan="2">T2D1 T2D1</td><td>z</td></tr>
<tr><td>A</td><td>A</td><td>B</td><td>0</td></tr>
<tr><td>B</td><td>A</td><td>C</td><td>0</td></tr>
<tr><td>C</td><td>C</td><td>B</td><td>0</td></tr>
<tr><td>D</td><td>C</td><td>B</td><td>1</td></tr>
</table></td><td>CO3</td><td>PO3</td><td>10</td></tr>
<tr><td></td><td></td><td>b)</td><td>Develop the state diagram and design a Mealy type FSM for a serial adder using D flip flops. Write the Verilog Code for the same</td><td>CO3</td><td>PO3</td><td>10</td></tr>
<tr><td></td><td></td><td></td><td>OR</td><td></td><td></td><td></td></tr>
</table>

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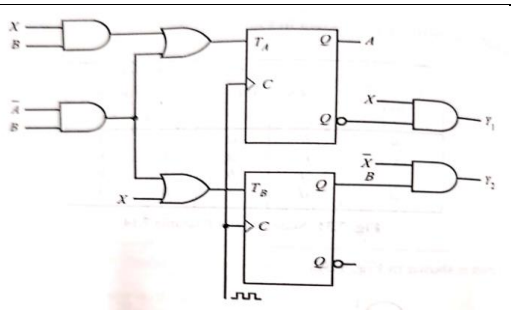
	8	a)	 Construct its transition table, excitation table, state table and the state diagram. Write Verilog code to realize the state machine.	*CO3*	*PO3*	**10**
		b)	Develop the state diagram and design a Moore type FSM for a serial adder using D flip flops. Write the Verilog Code for the same	*CO3*	*PO3*	**10**
			UNIT - V			
	9	a)	What is the role of FPGAs in ASIC market? Explain with neat diagrams, the architecture of Xilinx XC 4000 seires	*CO1*	*PO1*	**10**
		b)	Explain with a neat diagram the high level architecture of a CPLD	*CO1*	*PO1*	**10**
			OR			
	10	a)	What are PAL devices? With neat diagrams, explain the architecture of Altera 7000 series CPLD.	*CO1*	*PO1*	**10**
		b)	Implement the functions f1 and f2 using PLA of appropriate size. f1 = Σm (1,2,3,7) f2 = Σm (0,1,2,6). Draw PLA Table.	*CO1*	*PO1*	**10**

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