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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

June 2025 Semester End Main Examinations

Programme: B.E. **Semester: VI**

Branch: Electrical and Electronics Engineering **Duration: 3 hrs.**

Course Code: 23EE6PE2FV **Max Marks: 100**

Course: Fundamentals of VLSI

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT - I	***CO***	***PO***	**Marks**
1	a)	With neat sketches, explain the fabrication process of P-well CMOS Transistor.		*CO1*	*PO1*	**10**
	b)	Explain thermal sequence difference between NMOS and CMOS processes.		*CO1*	*PO1*	**05**
	c)	Explain the production of E-beam masks.		*CO1*	*PO1*	**05**
		OR				
2	a)	With neat sketches, explain the fabrication process of NMOS Transistor.		*CO1*	*PO1*	**10**
	b)	State and explain Moore's law.		*CO1*	*PO1*	**05**
	c)	Explain the various modes of operation of an NMOS enhancement mode transistor.		*CO1*	*PO1*	**05**
		UNIT - II				
3	a)	Derive the expressions for drain to source current I_{ds} versus voltage V_{ds} relationship in different operating regions.		*CO2*	*PO1*	**06**
	b)	Draw and explain briefly, the transfer characteristics of a CMOS inverter.		*CO2*	*PO2*	**08**
	c)	Explain Latch-up in CMOS circuits.		*CO2*	*PO1*	**06**
		OR				
4	a)	Derive the Pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter		*CO2*	*PO2*	**08**
	b)	Define i) Output Conductance ii) Transconductance		*CO2*	*PO1*	**06**
	c)	What is Body effect? Explain briefly MOS transistor threshold voltage and list the parameters on which it depends.		*CO2*	*PO1*	**06**

			UNIT - III			
	5	a)	Derive the expressions for CMOS inverter delay in terms of Rise time and Fall time.	*CO2*	*PO2*	**08**
		b)	Explain briefly Lambda based design rules for i) wires ii) Transistors	*CO2*	*PO1*	**06**
		c)	Draw the stick diagram and mask layout for an 8:1 NMOS inverter in NMOS design style.	*CO2*	*PO2*	**06**
			OR			
	6	a)	Find the expressions for NMOS inverter pair delay	*CO2*	*PO2*	**08**
		b)	Draw the stick diagram and mask layout for a 1:1 CMOS inverter in CMOS design style.	*CO2*	*PO2*	**06**
		c)	Explain briefly the effect of wiring capacitances in VLSI designs.	*CO2*	*PO1*	**06**
			UNIT - IV			
	7	a)	Find the scaling factors for i) Gate Area ii) Gate Capacitance iii) Energy stored in gate capacitance iv) Saturation Current	*CO3*	*PO2*	**08**
		b)	List the advantages of scaling. Define Scaling factor.	*CO3*	*PO1*	**06**
		c)	With the help of truth table, draw the Stick diagram of 2 input CMOS NOR gate and 2 input NMOS NOR Gate.	*CO3*	*PO2*	**06**
			OR			
	8	a)	Briefly describe the architecture issues that occur for system design process.	*CO3*	*PO1*	**06**
		b)	Find the scaling factors for v) Gate Delay vi) Frequency of operation vii) Power Dissipation per gate viii) Current Density	*CO3*	*PO2*	**08**
		c)	Explain briefly the limitations of scaling.	*CO3*	*PO1*	**06**
			UNIT - V			
	9	a)	Derive the expression for Zpu/Zpd for a Pseudo- NMOS Logic.	*CO4*	*PO2*	**10**
		c)	What is structured design? Design a parity generator using the structured approach.	*CO4*	*PO2*	**10**
			OR			
	10	a)	Design 4 to 1 multiplexer using switch logic.	*CO4*	*PO2*	**08**
		b)	Draw the stick diagram for 1-bit non inverting NMOS dynamic storage and hence explain the shift register.	*CO4*	*PO2*	**06**
		c)	Differentiate between Clocked CMOS logic and Dynamic CMOS logic.	*CO4*	*PO2*	**06**

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