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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## July 2023 Semester End Main Examinations

**Programme: B.E.** **Semester: VI**
**Branch: Electrical and Electronics Engineering** **Duration: 3 hrs.**
**Course Code: 19EE6PE3VL** **Max Marks: 100**
**Course: Circuit Design using VLSI** **Date: 17.07.2023**

**Instructions**: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

| | | UNIT - I | CO | PO | Marks |
|---|---|---|---|---|---|
| 1 | a) | Using the table given, plot the drain characteristics (For Vds=1.5V) for the NMOS enhancement transistor and indicate the 3 regions of operations. | *CO2* | *PO2* | **06** |

| Vds(V) | Ids(uA) |
|---|---|
| 0 | 0 |
| 0.5 | 30 |
| 1 | 100 |
| 1.5 | 220 |
| 2 | 400 |
| 2.5 | 620 |

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|---|---|---|---|---|---|
| | b) | Draw speed /power performance devices used in of VLSI technology. | *CO1* | *PO1* | **05** |
| | c) | List the steps involved in fabrication of NMOS transistor. Illustrate with neat diagram the fabrication. | *CO1* | *PO1* | **09** |
| | | **UNIT - II** | | | |
| 2 | a) | Illustrate the relationship between Ids versus Vds of a MOS under Linear and Saturation conditions. | *CO2* | *PO2* | **08** |
| | b) | Derive the expression for Zpu/Zpd ratio for an NMOS inverter driven by another NMOS Inverter. | *CO2* | *PO2* | **08** |
| | c) | What are the alternate forms of Pull-Ups? Which Pull Up is best suited for all applications in VLSI designs? | *CO1* | *PO1* | **04** |

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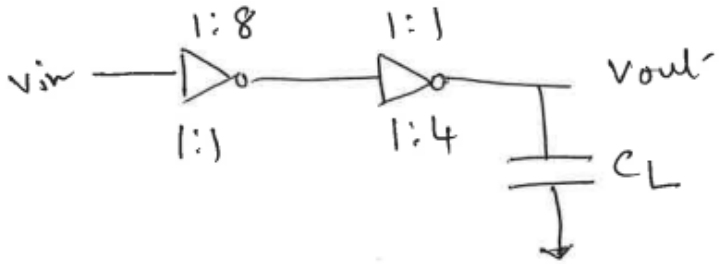
| | | | **UNIT - III** | | | |
| | 3 | a) | Consider the NMOS inverter as shown. Consider the capacitance at the output of Inverter 1 as 4 Cg and Load capacitance $C_L$ = 16 Cg. Calculate The total delay. Neglect stray capacitance.<br>  <br> | *CO2* | *PO2* | **06** |
| | | b) | Draw the stick diagram and Mask layout of a 4:1 NMOS inverter in NMOS design style. | *CO2* | *PO1* | **06** |
| | | c) | Derive the expression for Cascaded inverters as drivers for a CMOS inverter. What is the value of " f " in cascaded inverters which will minimize the overall delay. | *CO2* | *PO2* | **08** |
| | | | **UNIT - IV** | | | |
| | 4 | a) | Realize with the help of circuit diagram, stick diagram and truth table a two Input NOR gate using i) NMOS ii) CMOS | *CO3* | *PO1* | **10** |
| | | b) | Derive the scaling factor for the following parameters in combined scaling:<br>i) Gate Delay<br>ii) Saturation Current<br>iii) Area capacitance<br>iv) Power speed product<br>v) Maximum Frequency of operation | *CO3* | *PO2* | **10** |
| | | | **OR** | | | |
| | 5 | a) | Derive the scaling factor for the following parameters in combined scaling:<br>i) Energy stored in gate capacitance<br>ii) Gate Capacitance<br>iii) Current Density | *CO3* | *PO2* | **06** |
| | | b) | Derive the expression for scaling of substrate doping concentration and width of depletion layer as applied to scaling factor. | *CO3* | *PO2* | **08** |
| | | c) | Realize with the help of circuit diagram, stick diagram and truth table a two Input NAND gate using NMOS transistor | *CO3* | *PO1* | **06** |
| | | | **UNIT - V** | | | |
| | 6 | a) | Explain Pseudo NMOS logic and derive the expression for Zpu/Zpd. | *CO4* | *PO1* | **10** |

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|---|---|---|---|---|---|---|
| | | b) | Describe Dynamic storage. Illustrate with stick diagrams the NMOS & CMOS<br>i) Basic inverting dynamic storage cells<br>ii) Basic non- inverting dynamic storage cells | *CO4* | *PO1* | **10** |
| | | | **OR** | | | |
| | 7 | a) | What are the various types of CMOS logic. Explain with block/circuit diagram, i) clocked CMOS ii) CMOS domino logic | *CO4* | *PO1* | **10** |
| | | b) | Explain with circuit diagram and stick diagram the working of a basic one bit cell NMOS parity generator. | *CO4* | *PO2* | **10** |

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