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B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

May 2023 Semester End Main Examinations

Programme: B.E.	**Semester: III**
Branch: Electronics and Communication Engineering	**Duration: 3 hrs.**
Course Code: 22EC3PCAEC	**Max Marks: 100**
Course: Analog Electronic Circuits	**Date: 15.05.2023**

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Determine the voltage V_{CEQ} and I_{CQ} for the voltage divider configuration of the circuit shown in figure 1 **10**

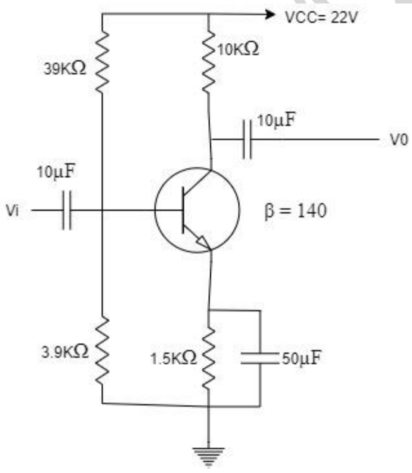

Figure 1

b) Draw the r_e model for a voltage divider bias configuration and derive expressions for input impedance, output impedance and voltage gain. **10**

UNIT - II

2 a) A transformer coupled class A power amplifier supplies power to 80Ω load connected across the secondary of a step down transformer having a turns ratio of 5:1. Determine the maximum power output for a zero signal collector current of 120mA **06**

b) With a neat block diagram derive expressions for gain with feedback, input impedance and output impedance for voltage series feedback configuration. **08**

c) Calculate the total harmonic distortion for an output signal having fundamental amplitude of 2.5V, second harmonic amplitude of 0.25V, third harmonic amplitude of 0.1V and fourth harmonic amplitude of 0.05V . **06**

UNIT - III

3 a) Derive an expression for drain current of NMOS transistor that operates in **10**
i) Triode region ii) Saturation region.

b) For the circuit shown in Figure 2, let Q1 and Q2 have Vt=0.6V, $\mu_n Cox=200\mu A/V^2$,L1=L2=0.8μm , W1 =8μm **10**
i) Find the value of R required to establish a current of 0.2mA in Q1
ii) Find W2 and a new value of R2 so that Q2 operates in saturation region with a current of 0.5mA and a drain voltage of 1V.

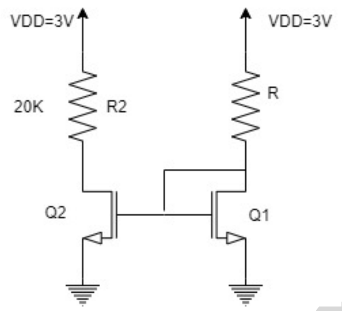

Figure 2

OR

4 a) Design the circuit shown in the Figure.3 so that the MOSFET operates at I_D=0.4mA and V_D = +0.5V. The NMOS transistor has Vt = 0.7v , μ_n Cox =100 $\mu A/V^2$ L=1 μm and W =32 μm. Neglect the channel length modulation effect (assume λ =0). **10**

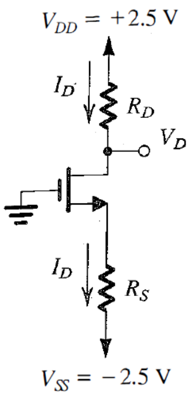

Figure 3

b) Describe different types of biasing in MOS amplifier circuits. **10**

UNIT - IV

5 a) Derive an expression for transconductance and voltage gain of a common source NMOS amplifier. **10**

b) Derive an expression for i) input impedance ii) output impedance iii) voltage gain and overall voltage gain for a common source amplifier with source resistance. **10**

UNIT - V

6 a) Find Vo for the circuit shown in figure 4. **10**

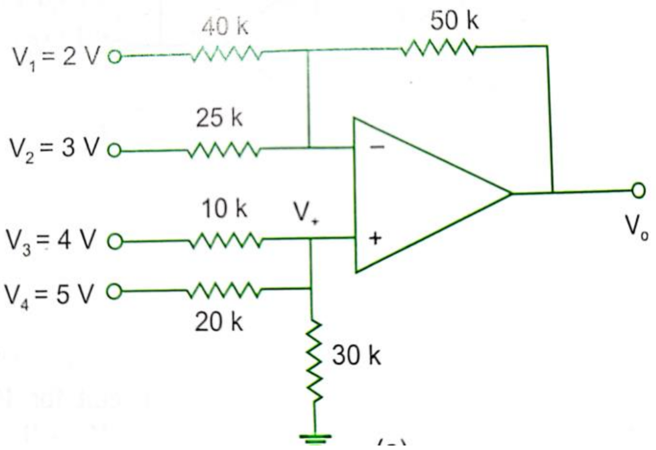

Figure 4

b) With a neat functional diagram describe the working of 555 Timer for astable operation. **10**

OR

7 a) Describe the basic operation of Phase Locked Loop(PLL). **10**

b) Design an adder circuit using an Opamp to obtain the output expression as: Vo= -[(0.4V 1 +0.1V 2 +20V 3)]. **04**

c) Describe the use of 555 Timer as Schmitt trigger. **06**

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