U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

December 2023 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCAEC **Max Marks: 100**
Course: Analog Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

UNIT - I

1 a) Identify the type of clipper, analyse the given circuit and represent the waveforms. **05**

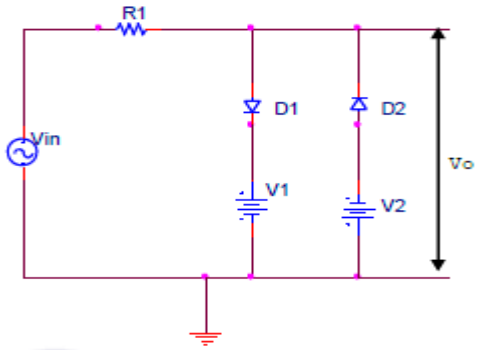

Fig-1

b) Design a suitable circuit represented by the box shown below which has the input and output waveforms as indicated for a frequency of 1KHz . **05**

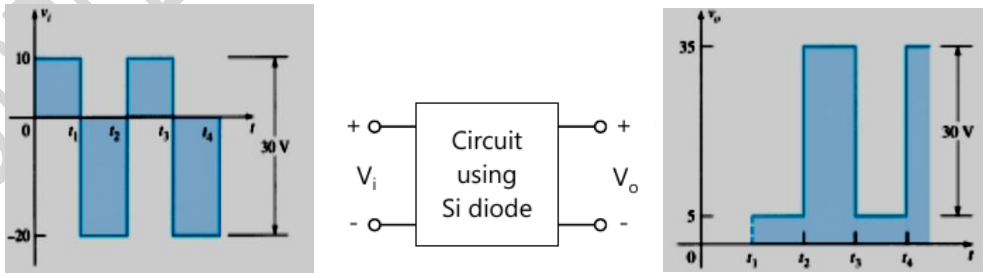

Fig-2

c) Explain frequency response of BJT RC coupled amplifier. Derive expression for higher cut off frequency considering the effect of device capacitors, miller capacitance and parasitic/stray wiring capacitors. **10**

UNIT - II

2 a) Identify the feedback mechnism in Fig3. Deduce an expression for gain,input impedance and output impedance for the same. **08**

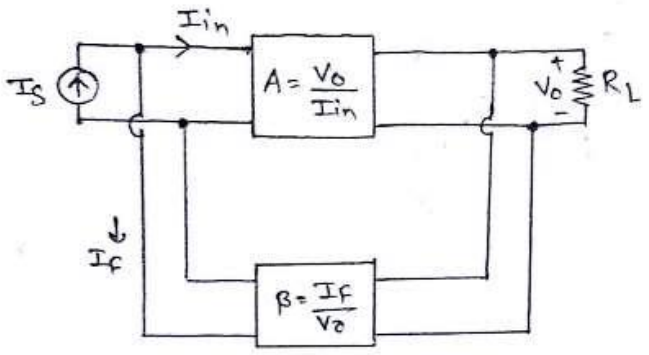

Fig-3

b) Determine the transformer turns ratio required to match a 16Ω speaker load so that the effective load resistance seen at the primary is 10 kΩ. **04**

c) Deduce an expression for efficiency of a Class B power amplifier.What are the drawbacks of the same? **08**

UNIT - III

3 a) Briefly describe the working of an enhancement type MOSFET under following conditions: **10**

i) With application of Small V_{DS}

ii) Operation of the device as V_{DS} is increased

b) Design the circuit shown in the fig 4 such that the transistor operates at I_D=0.4mA and V_D=0.5V.The NMOS transistor has V_t=0.7V,kn=100μA/V^2,L=1μm and W=32μm.Assume λ=0 **10**

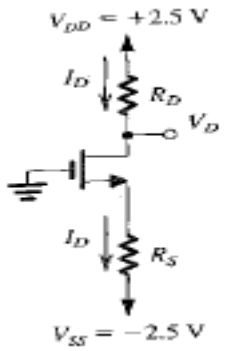

Fig-4

OR

4 a) With the help of neat cross sectional view describe the structure of a CMOS. **05**

b) Illustrate the significance of biasing a MOSFET using drain to gate feedback resistor. **05**

c) Consider an n-channel MOSFET with tox = 20 nm, μ_n = 650 cm2/V · s, Vt = 0.8 V, and W/L = 10. Find the drain current in the following cases: **10**

(a) V_{GS} = 5 V and V_{DS} = 1 V.

(b) V_{GS} = 2 V and V_{DS} = 1.2 V.

(c) V_{GS} = 5 V and V_{DS} = 0.2 V.

(d) V_{GS}= V_{DS} = 5 V.

UNIT - IV

5 a) Deduce an expression for small signal voltage gain of an enhancement MOSFET as an amplifier. **10**

b) With supportive diagrams derive an expression for overall voltage gain of a grounded gate amplifier. **10**

UNIT - V

6 a) Briefly describe the working of the differential pair in Common Mode and Differential Mode. **10**

b) Determine the output Vo for the Adder-Subtractor circuit shown in Fig-5. Represent the equivalent circuits at each stage. **10**

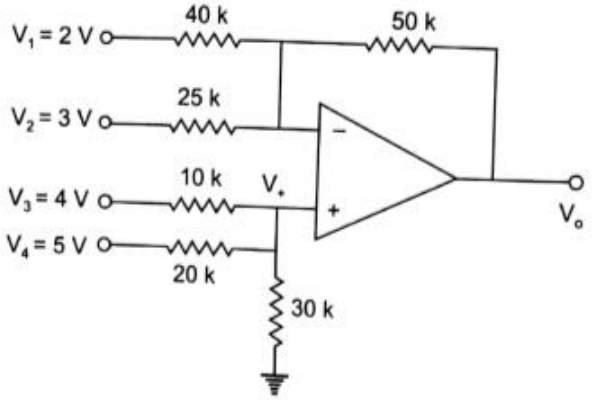

Fig 5

OR

7 a) It is required to convert a voltage signal to a proportional output current for a certain application. Suggest and describe the different types of converters with necessary equations and circuits. **10**

b) Suggest a suitable circuit to generate a symmetric square wave generator. Deduce an expression for the total time period for the same. **10**

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