U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

Autonomous Institute Affiliated to VTU

September / October 2024 Supplementary Examinations

Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCAEC **Max Marks: 100**
Course: Analog Electronic Circuits

Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

UNIT - I

1 a) Draw the transfer characteristics for basic parallel clipper with positive clipping, using reference voltage V_R. Let the cut in voltage of the diode be V_γ. **04**

b) With relevant equations analyze voltage divider bias circuit using exact analysis approach. **10**

c) Draw a small signal model for the circuit shown in fig 1c and derive an expression for voltage gain and input impedance. **06**

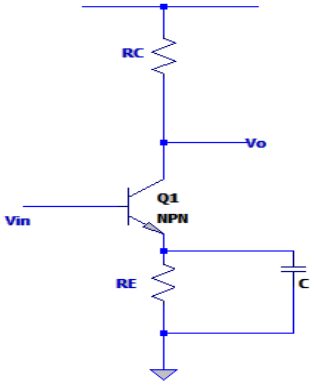

Fig 1c

UNIT - II

2 a) Derive an expression for input and output impedance with feedback for a current shunt feedback amplifier. **06**

b) For the voltage series feedback amplifier shown in fig 2b, find R_{if}, A_f, R_{of}. Let R_{id}=200KΩ, R_L=30 KΩ, μ=10^3, r_0=5 KΩ, R_S= 10 KΩ. **10**

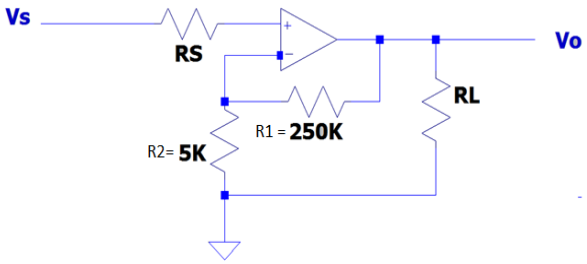

Fig 2b

c) Prove with a neat circuit diagram the efficiency of a transformer coupled amplifier is 50%. **04**

UNIT - III

3 a) Derive an expression for drain current in linear region and saturation region for a nMOS transistor. **06**

b) Find R_1, R_2, R_d and maximum R_d to operate the device in saturation for the circuit shown in fig 3b. **10**

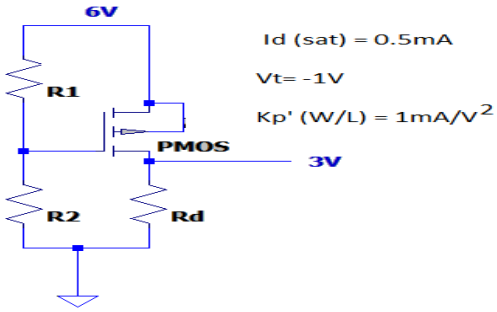

Fig 3b

c) Find R_D and R_S for the circuit shown in fig 3c. Assume $I_D = 0.5mA$, $V_t = 0.8V$, $\mu_n C_{ox} = 200\mu A/V^2$, $\frac{W}{L} = 20$ **04**

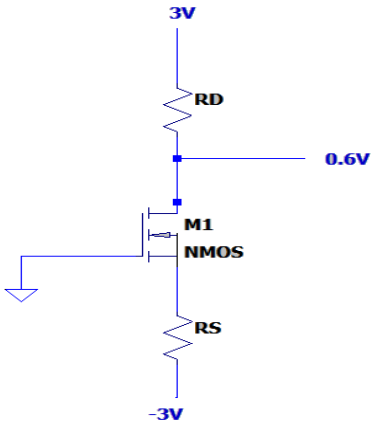

Fig 3c

OR

4 a) Explain the working of nMOS transistor under the following voltage conditions: **06**

(i) $V_{GS} < V_t$

(ii) $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$

(iii) $V_{GS} > V_t$ and $V_{DS} > (V_{GS} - V_t)$

b) Find I_{Dp}, I_{Dn} and V_0 for the circuit shown in fig 4b when (i) Vi= 0V (ii) Vi=2.5V (iii) Vi= - 2.5V. Let $k_n'(W/L)n = k_p'(W/L)p = 1mA/V^2$, $V_{tn} = -V_{tp} = 1V$. **10**

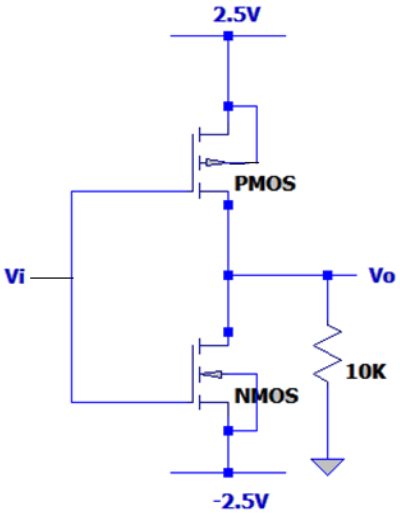

Fig 4b

c) Write a note on MOS conducting in sub threshold region. **04**

UNIT - IV

5 a) Find I_D, g_m, $\frac{Vo}{Vi}$, R_i, $\frac{Vo}{Vs}$ and R0 for the circuit shown in fig 5a. Let $k_n'(W/L)$ = 1.2 mA/V^2, V_t = 0.5V and λ=0. **10**

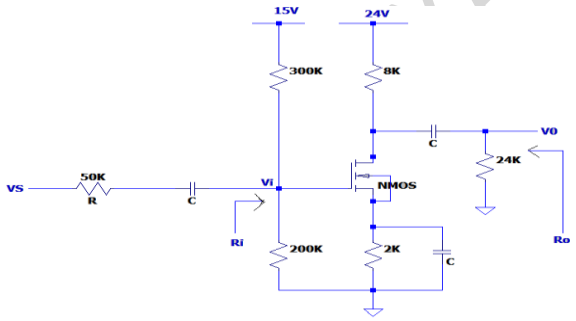

Fig 5a

b) Draw a circuit of Wilson MOS mirror and derive an expression for output impedance. **10**

UNIT - V

6 a) Design a low and high voltage regulator using IC723. **10**

b) Design an instrumentation amplifier circuit, to provide a gain that can be varied over the range of 2 to 1000 utilizing a 100 KΩ variable resistance. **10**

OR

7 a) With a neat circuit explain shunt regulator using Opamp. List its limitations. **10**

b) Suggest a suitable circuit to generate a symmetric square wave generator. Deduce an expression for the total time period for the same. **10**

******