U.S.N.										

B.M.S. College of Engineering, Bengaluru-560019

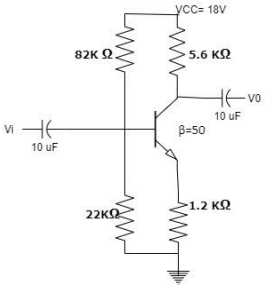
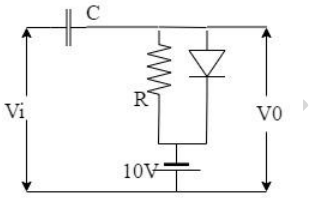
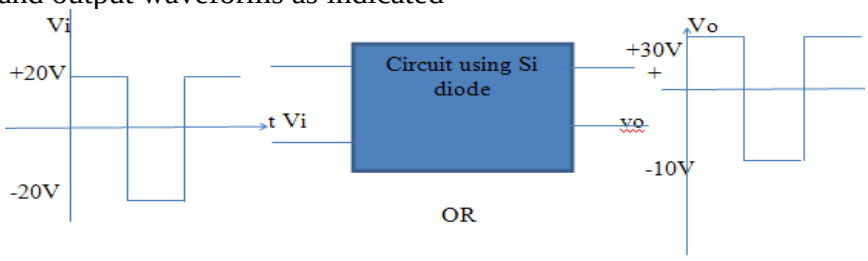
Autonomous Institute Affiliated to VTU

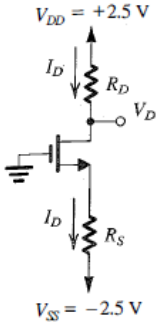
January / February 2025 Semester End Main Examinations

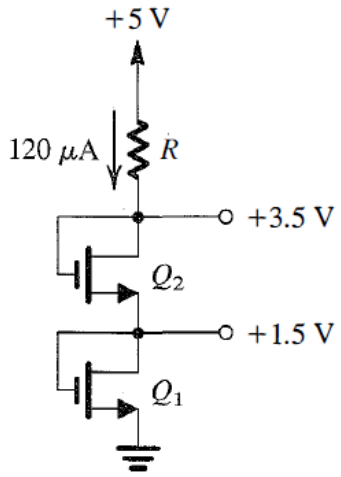
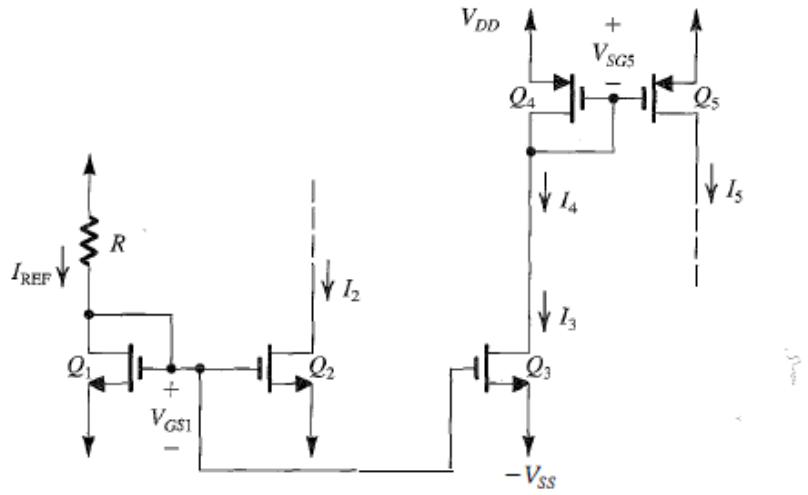
Programme: B.E. **Semester: III**
Branch: Electronics and Communication Engineering **Duration: 3 hrs.**
Course Code: 22EC3PCAEC **Max Marks: 100**
Course: Analog Electronic circuits

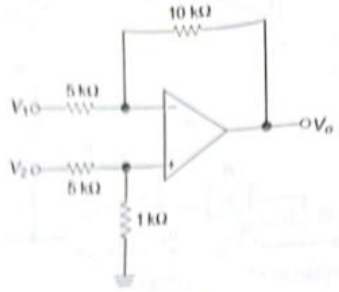
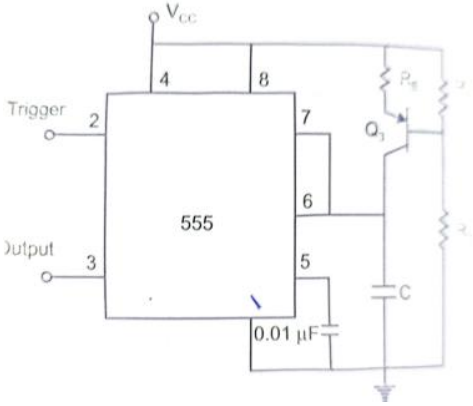
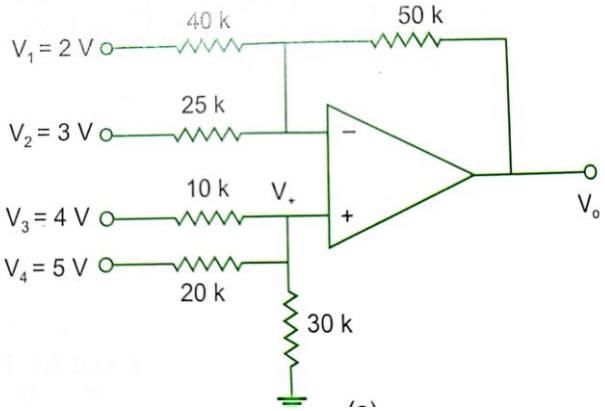
Instructions: 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

Important Note: Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

			UNIT – I	CO	PO	Marks
1	a)		Determine the levels of I_{CQ} and V_{CEQ} for the voltage divider bias circuit shown in the figure 1  Figure 1	*CO 2*	*PO 1*	**6**
	b)		Analyze the circuit shown in Figure 2 and sketch the input and ouput voltage waveform assuming an ideal diode. (Vi =20sinωt)  Figure 2	*CO3*	*PO2*	**06**
	c		Draw the r_e model for a voltage divider bias configuration and derive expressions for input impedance, output impedance and voltage gain.	*CO2*	*PO1*	**08**
			OR			
2	a)		Design a suitable circuit for the block shown below which has input and output waveforms as indicated  OR	*CO3*	*PO2*	**8**

		b)	Explain the working of voltage divider bias circuit using approximate analysis and for the voltage divider bias configuration having R_1=33KΩ, R_2=8.6KΩ, R_C=3.9KΩ, R_E=1.2KΩ, V_{CC}=20V, β=110. Calculate V_B, I_B, V_E, V_{CE}	*CO2*	*PO1*	**12**
			UNIT II			
	3	a)	With a neat block diagram derive expressions for gain with feedback, input impedance and output impedance for current series feedback configuration	*CO2*	*PO1*	**06**
		b)	A class B power amplifier output stage is required to deliver an average power of 100W into a 16 Ω load. The power supply should be 4V greater than the corresponding peak sine-wave output voltage. Determine the power supply voltage required (to the nearest volt in the appropriate direction),the peak current from each supply, the total supply power, and the power conversion efficiency .Also determine the maximum possible power dissipation in each transistor for a sinewave input .	*CO2*	*PO2*	**10**
		c)	Derive an expression for miller effect induced input and output capacitance for an inverting amplifier	*CO2*	*PO1*	**04**
			OR			
	4	a)	Suggest a suitable method to increase the efficiency of series fed Class A Power Amplifier and deduce an expression to prove the efficiency is higher than Series fed Class A type.	*CO2*	*PO1*	**8**
		b)	Determine the voltage gain, input and output impedance with feedback for voltage series feedback having A=90, Ri=15KΩ, Ro=20KΩ for feedback of: i) β=-0.2 ii) β=-0.75	*CO3*	*PO3*	**6**
		c)	Calculate the total harmonic distortion for an output signal having fundamental amplitude of 2.5V, second harmonic of amplitude 0.25, third harmonic amplitude of 0.1V and fourth harmonic amplitude of 0.05V	*CO3*	*PO3*	**6**
			UNIT - III			
	5	a)	Design the circuit of Figure 3 so that the transistor operates at I_D = 0.4 rnA and V_D= +0.5V . The NMOS transistor has Vt= 0.7 V, μnCox = 1 00 μA/V^2, L= 1μm, and W= 32μm. Neglect the channel-length modulation effect (i.e., assume that λ=0).  Figure 3	*CO4*	*PO3*	**10**
		b)	Discuss the need for biasing MOS amplifiers. Describe different types of biasing in MOS amplifier circuits.	*CO1*	-	**10**

			OR			
	6	a)	Derive an expression for the drain current of NMOS transistor operating in (i) Triode region and (ii) Saturation region	*CO2*	*PO1*	**10**
		b)	The NMOS transistors in the circuit of Fig. 4 have Vt, == 1 V, μnCox == 120 μA/v², λ= 0, and LI == L2 = 1 μm. Find the required values of gate width for each of QI and Q2, and the value of R, to obtain the voltage and current values indicated.  Figure 4	*CO3*	*PO2*	**10**
			UNIT – IV			
	7	a)	Derive an expression for i) input impedance ii)output impedance iii)voltage gain and overall voltage gain for a common source amplifier with source resistance	*CO2*	*PO1*	**10**
		b)	Identify the circuit shown in the figure 5, explain its significance in biasing the MOS amplifier  Figure 5	*CO3*	*PO2*	**10**
			OR			
	8	a)	Develop the T equivalent circuit model for the MOSFET, draw the necessary diagrams and explain.	*CO3*	*PO2*	**8**
		b)	Derive the expression for input resistance, output resistance, voltage gain and overall voltage gain of a common gate MOSFET amplifier	*CO2*	*PO2*	**12**

			UNIT – V			
	9	a)	Find the output voltage V0 for the circuit given in Figure 6.  Figure 6	*CO2*	*PO1*	**10**
		b)	Identify the circuit shown in figure 7, with appropriate mathematical analysis determine the kind of output generated.  Figure 7	*CO3*	*PO3*	**10**
			OR			
	10	a)	Using a neat block diagram explain the working of Phase locked loop	*CO1*	-	**10**
		b)	Find Vo for the circuit shown in figure 8  Figure 8	*CO2*	*PO1*	**10**

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