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# B.M.S. College of Engineering, Bengaluru-560019

**Autonomous Institute Affiliated to VTU**

## August 2023 Semester End Make-Up Examinations

**Programme: B.E.** **Semester: III**
**Branch: Electronics and Communication Engineering** **Duration: 3 hrs.**
**Course Code: 22EC3PCAEC** **Max Marks: 100**
**Course: Analog Electronic Circuits** **Date: 17.08.2023**

**Instructions:** 1. Answer any FIVE full questions, choosing one full question from each unit.
2. Missing data, if any, may be suitably assumed.

**Important Note:** Completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages. Revealing of identification, appeal to evaluator will be treated as malpractice.

### UNIT - I

1 a) What is Transistor biasing? Mention the requirements for biasing a transistor. **05**

b) Draw the circuit diagram of common Emitter voltage divider bias configuration and derive the expression for input impedance, output impedance, voltage gain and current gain, using $r_e$ model. **08**

c) Determine the dc bias voltage $V_{CE}$ and the current $I_C$ for the voltage divider bias configuration given $R_1$ =39 kΩ, $R_2$ =10 kΩ, $R_C$ =3.9 kΩ, $R_E$ = 1.5 kΩ, $V_{CC}$ = 22V and β = 100. Assume Si transistor. **07**

### UNIT - II

2 a) With a neat circuit diagram, explain the operation of complementary symmetry Class B push-pull amplifier and show that its maximum conversion efficiency is 78.5%. **06**

b) A transformer-coupled class A amplifier drives a 16 Ω speaker through a 3.87:1 transformer. Using a power supply of $V_{CC}$ = 36 V, the circuit delivers 2 W to the load. Calculate: (i) $P_{(ac)}$ across transformer primary. (ii) $V_{L(ac)}$. (iii) $V_{(ac)}$ at transformer primary. (iv) The rms values of load and primary current. **04**

c) Obtain the expression for gain, input resistance and output resistance for a voltage series feedback amplifier. **10**

### UNIT - III

3 a) Explain the structure of enhancement type MOSFET and its operation. **12**

b) Determine the values of $R_S$ and $R_D$ for the circuit shown in fig 1 so that the transistor operates at $V_{DD} = -V_{SS} = 2.5V$, $I_D = 0.3$ mA and $V_D = +0.4$ V. The NMOS transistor has $V_t = 1$ V, $\mu_n C_{ox} = 60\ \mu A/V^2$ and W/L = 40. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$). **08**

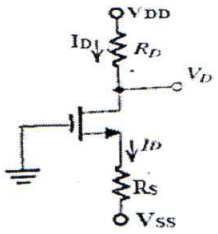


fig 1

**OR**

4 a) Write short notes on (i) Complementary MOS (ii) MOSFET amplifier configurations. **10**

b) State the disadvantages of fixed $V_{GS}$ biasing technique and explain how stability of operating point is achieved in drain to gate feedback resistor biasing technique in a MOSFET amplifier. **10**

**UNIT - IV**

5 a) Analyze the circuit of common drain amplifier and derive the expressions for no-load voltage gain, overall voltage gain, input resistance and output resistance. **08**

b) For the circuit shown in figure 2, derive the expression for $R_{in}$, Ro, $A_V$ and $A_{VO}$ using T- Model. **06**

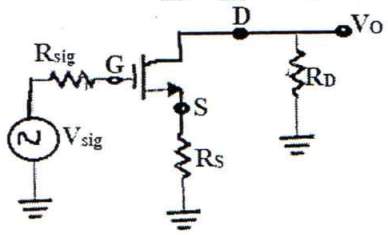


Figure 2

c) Explain the operation of Wilson MOS Mirror. **06**

**UNIT - V**

6 a) With a neat circuit diagram and relevant equations, explain the operation of instrumentation amplifier. **08**

b) Implement the equation $V_O = 3V_1 + 6V_2 - V_3$ using inverting op-amps. **06**

c) Show how op-amp can be used as a logarithmic amplifier. **06**

**OR**

7 a) With a neat block diagram explain the operation of PLL. Also define (i) Lock-in range (ii) Pull in time (iii) Capture range. **08**

b) Mention the important characteristics and explain the performance parameters of three terminal IC regulators. **07**

c) Design an Astable multivibrator using 555 timer to provide output frequency of 1 kHz with a duty cycle of 60%. The capacitor used has a nominal value of 0.1μF. **05**

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